NEWHAVEN DISPLAY INTERNATIONAL

Product Specification

NHD-6.8-4801280AF-ASXP

TFT Liquid Crystal Display

NHD-	Newhaven Display
6.8-	6.8" Diagonal
480128-	480xRGBx1280 Pixels
AF-	Model
A-	Built-in Driver / No Controller
S-	High Brightness, White LED Backlight
X-	TFT
P-	IPS, Wide Temperature

Newhaven Display International, Inc.
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REACH Compliant

RoHS Compliant

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Table of Contents

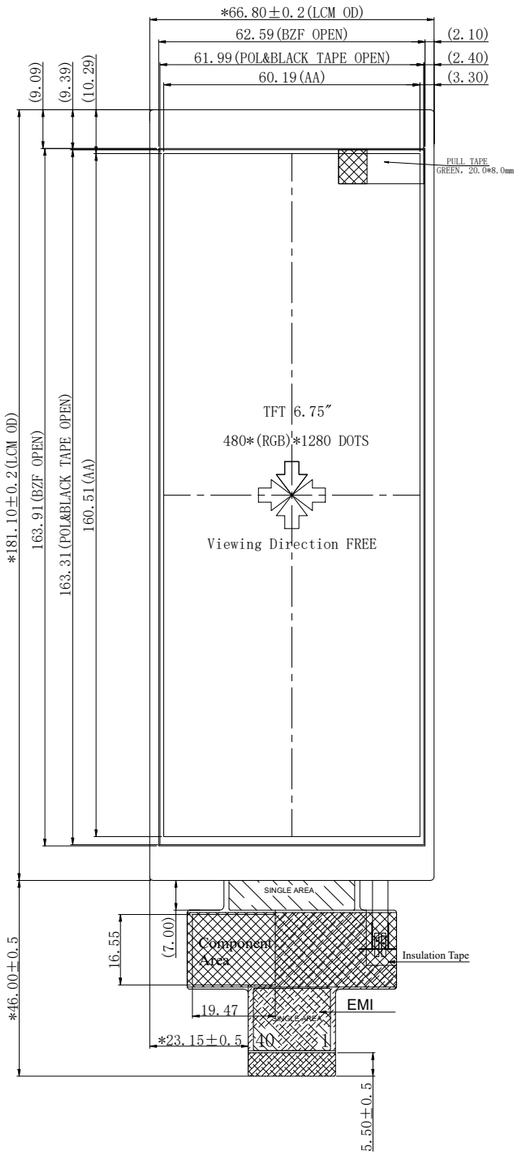
Additional Resources

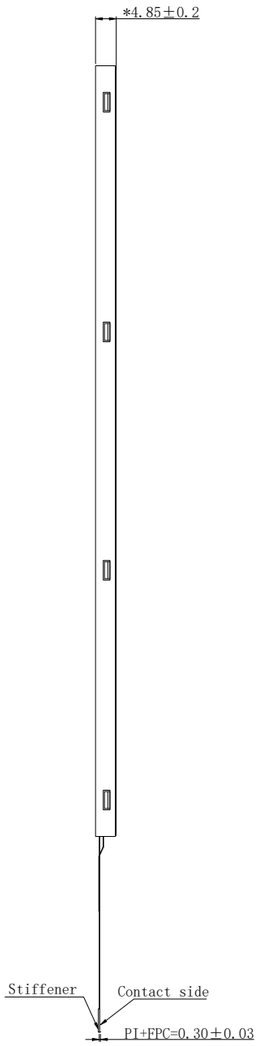
- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

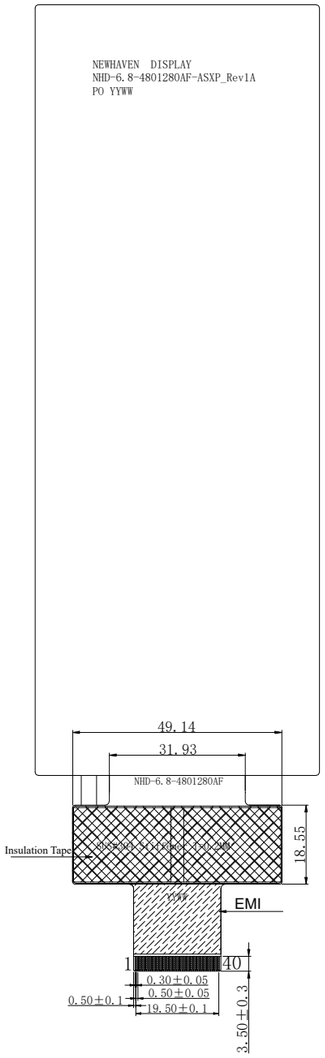
Document Revision History

Revision	Date	Description	Changed By
-	03/09/2026	Initial Release	JT

Mechanical Drawing



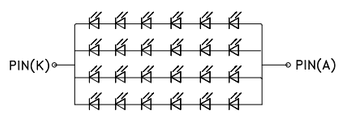




PIN	SYMBOL
1	LED_K
2	LED_A
3	NC
4	VCC
5	GND
6	MIPI_DON
7	MIPI_DOP
8	GND
9	MIPI_D1N
10	MIPI_D1P
11	GND
12	MIPI_CLKN
13	MIPI_CLKP
14	GND
15	SPI_CSX
16	SPI_SCL
17	SPI_SDI
18	SPI_SDO
19	TE
20	RESX
21	IMO
22	BIST_EN
23	GND
24	LVDS_DOP
25	LVDS_DON
26	GND
27	LVDS_D1P
28	LVDS_D1N
29	GND
30	LVDS_CLKP
31	LVDS_CLKN
32	GND
33	LVDS_D2P
34	LVDS_D2N
35	GND
36	LVDS_D3P
37	LVDS_D3N
38	GND
39	NC
40	VPP_OTP

Product Description: 6.8” 480x1280 IPS TFT

1. Driver IC: NV3051F-L
2. Interface: 2-lane MIPI DSI, LVDS
3. Power Requirement: 3.3V TFT, 18V/170mA Backlight
4. Optical Features: Normally Black, Transmissive, Anti-Glare, 1200cd/m²
5. Recommended FFC Connector: 40pin 0.5mm pitch; Molex 54132-4062
6. Built-in EMI Shielding



LED CIRCUIT DIAGRAM

Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

Drawing/Part Number: NHD-6.8-4801280AF-ASXP
Revision: 1A

Unless otherwise specified:
• Dimensions are in Millimeters
• Third Angle Projection

Drawn By: K. Lewis
Approved By: K. Lewis
Drawn Date: 03/09/2026
Approved Date: 03/09/2026

Pin Description

Pin No.	Symbol	External Connection	Function Description
1	LED_K	LED Power Supply	Backlight Cathode (Ground)
2	LED_A	LED Power Supply	Backlight Anode (170mA @ 18V)
3	NC	-	No Connect
4	V_{DD}	Power Supply	Power Supply for LCD and Logic (3.3V)
5	GND	Power Supply	Ground
6	MIPI_D0N	MPU	MIPI DSI Differential Data Negative input Lane 0
7	MIPI_D0P	MPU	MIPI DSI Differential Data Positive input Lane 0
8	GND	Power Supply	Ground
9	MIPI_D1N	MPU	MIPI DSI Differential Data Negative input Lane 1
10	MIP_D1P	MPU	MIPI DSI Differential Data Positive input Lane 1
11	GND	Power Supply	Ground
12	MIPI_CLKN	MPU	MIPI DSI Differential Clock Negative input
13	MIPI_CLKP	MPU	MIPI DSI Differential Clock Positive input
14	GND	Power Supply	Ground
15	SPI_CSX	MPU	Active LOW Chip Select signal
16	SPI_SCL	MPU	Serial Clock signal
17	SPI_SDI	MPU	Serial Data Input
18	SPI_SDO	MPU	Serial Data Output
19	TE	MPU	Tearing Effect Output
20	RESX	MPU	Active LOW Reset signal
21	IM0	MPU	Polarity and Data Lane Swap signal
22	BIST_EN	MPU	Built in Self-Test BIST = H: Self- Test Enabled BIST = L: Normal Operation
23	GND	Power Supply	Ground
24	LVDS_D0P	MPU	LVDS Differential Data Positive input CH0
25	LVDS_D0N	MPU	LVDS Differential Data Negative input CH0
26	GND	Power Supply	Ground
27	LVDS_D1P	MPU	LVDS Differential Data Positive input CH1
28	LVDS_D1N	MPU	LVDS Differential Data Negative input CH1
29	GND	Power Supply	Ground
30	LVDS_CLKP	MPU	LVDS differential Clock Positive input
31	LVDS_CLKN	MPU	LVDS differential Clock Negative input
32	GND	Power Supply	Ground
33	LVDS_D2P	MPU	LVDS Differential Data Positive input CH2
34	LVDS_D2N	MPU	LVDS Differential Data Negative input CH2
35	GND	Power Supply	Ground
36	LVDS_D3P	MPU	LVDS Differential Data Positive input CH3
37	LVDS_D3N	MPU	LVDS Differential Data Negative input CH3
38	GND	Power Supply	Ground
39	NC	-	No Connect
40	VPP_OTP	-	**Don't Use – Leave as No Connect**

Recommended LCD connector: 0.5mm pitch 40-Conductor FFC. Molex p/n: 54132-4062 or similar

NOTE: When using MIPI, display must be initialized via SPI before sending pixel data. SPI cannot be used for pixel data.

Polarity and Data Lane Selection

IM0	D0P/N	D1P/N	CLKP/N
0	D0P/N	D1P/N	CLKP/N
1	D0N/P	D1N/P	CLKN/P

Internal Registers

The NV3051F-L driver supports high speed serial interface, MIPI to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. Updating command instructions can also be accomplished by using all supporting system interfaces.

The NV3051F-L driver has the following major categories of instructions:

- System function instructions (User Command Set).
- Customer Command List and Description (Manufacturer Command Set / Command 2).

Since updating these instructions are asynchronous to the internal clock of the NV3051F-L driver, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents will describe the supported instructions in detail:

- System function commands

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state (Please refer to “RESET TABLE” section). The commands 10h, 11h, 20h, 21h, 22h, 23h, 28h, 29h, 36h will be updated only during V-sync periods while module is in the “Sleep Out” mode to avoid abnormal visual effects and will be updated immediately in the “Sleep In” mode. The Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh), and Read Display Self Diagnostic Result (0Fh) will be updated immediately in both “Sleep In” and “Sleep Out” mode

System function command accessing flow is described as the following example.

Example 1: Sleep Out
CMDWR 0x11

Example 2: Display On
CMDWR 0x29

Example 3: TE ON
CMDWR 0x35
DATWR 0x00

SPI Interface Mode

NV3051F-L driver requires SPI to initialize the display before sending pixel data over MIPI. SPI cannot be used for sending pixel data.

The serial interface is used to communicate between the microcontroller and the LCD driver chip. It contains CSX (chip select), SCL (serial clock), SDI (serial data input) and SDO (serial data output). Serial clock (SCL) is used for interface with MPU only, so it can be stopped when no communication is necessary. If the host places the SDI line into high-impedance state during the read intervals, then the SDI and SDO can be tied together.

SPI Write Mode

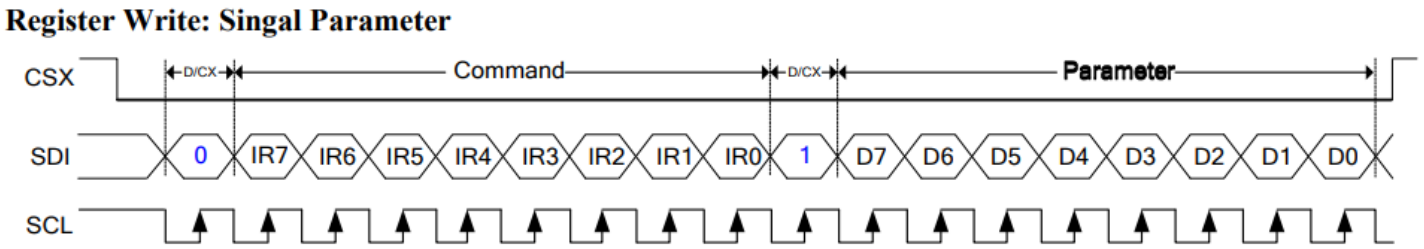


Figure: SPI Protocol for write

SPI Read Mode

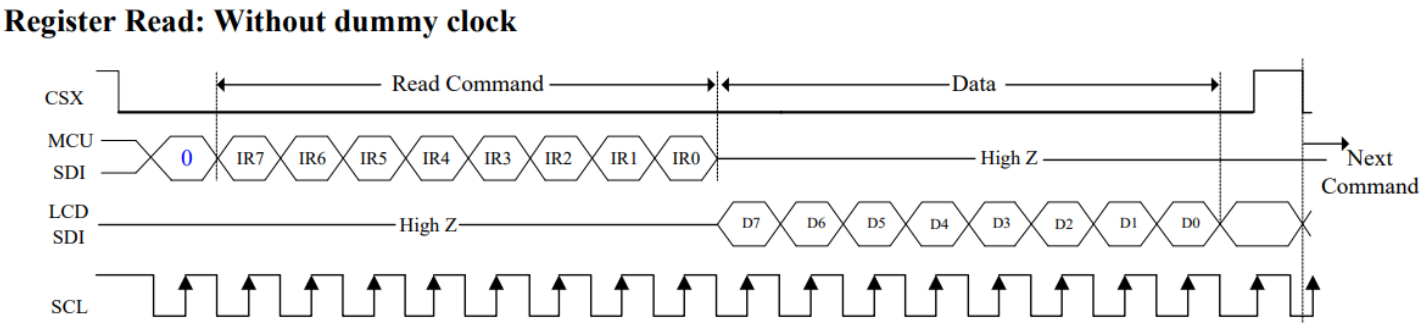


Figure: SPI Protocol for register read mode

MIPI DSI Interface Mode

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.
Vsync (VS) indicates the beginning of each frame of the displayed image.
Hsync (HS) signals the beginning of each horizontal line of pixels.
Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data.
Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

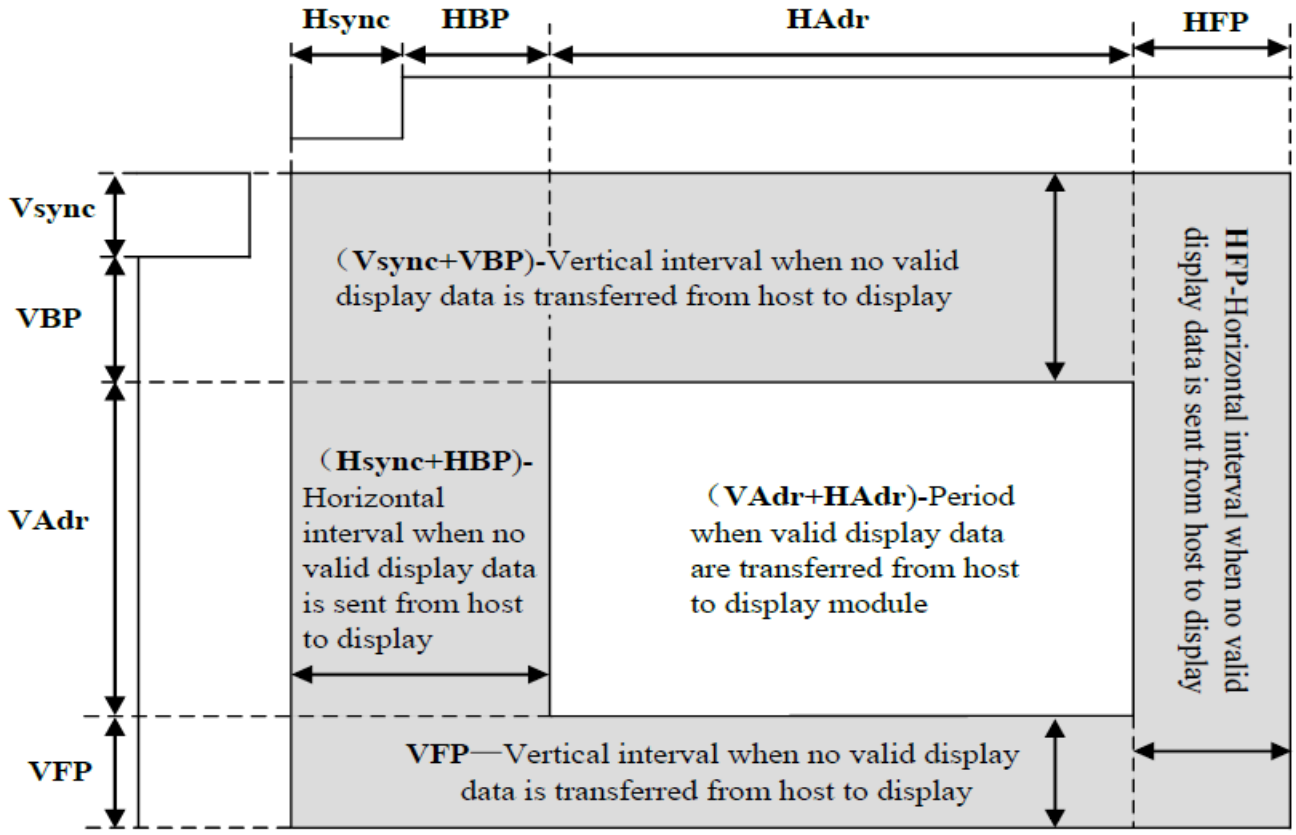


Figure define timing parameter for MIPI video operation

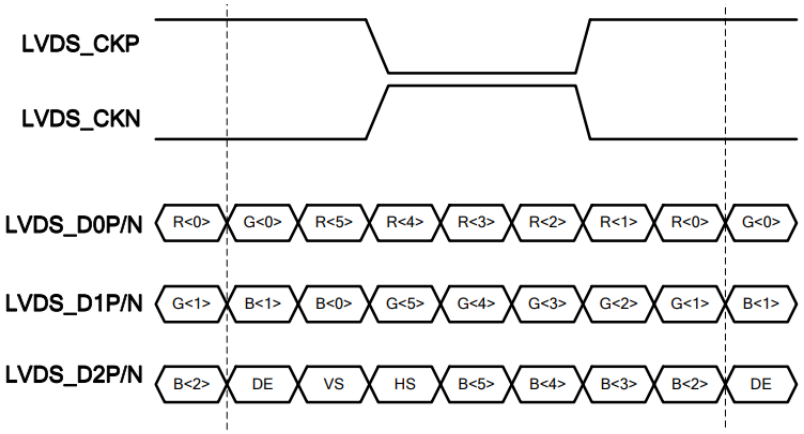
The NV3051F-L driver's MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00.

Recommended Timing Values

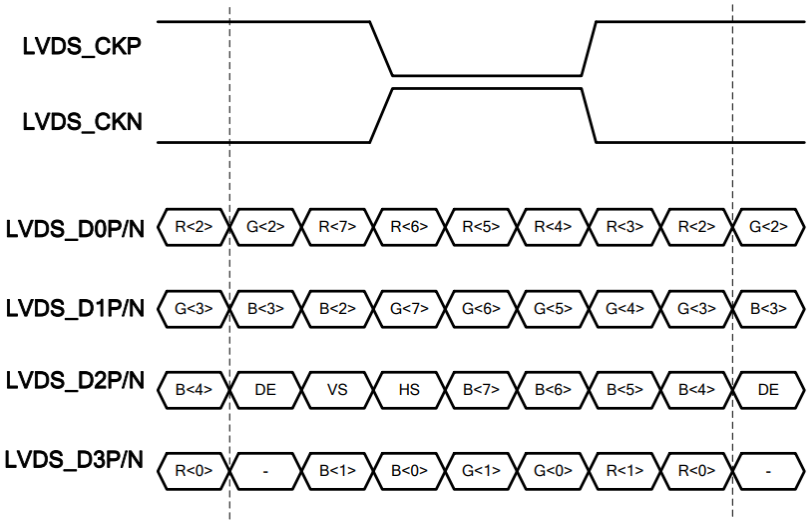
HS Total	HFP	HBP	HS Pulse	VS Total	VFP	VBP	VS Pulse	PCLK Freq
600	46	44	2	1280	16	8	2	54 MHz

LVDS Interface Mode

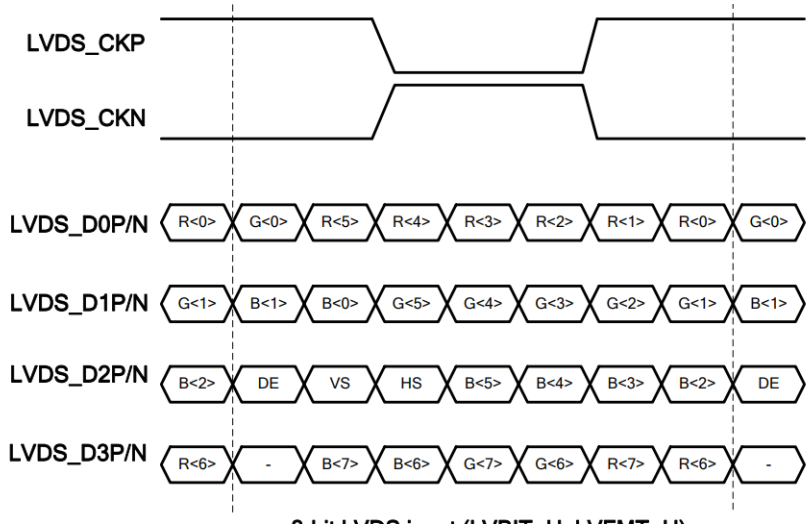
Data Input Format



6-bit LVDS input (LVBIT=L, LVFMT=Don't care)



8-bit LVDS input (LVBIT=H, LVFMT=L)



8-bit LVDS input (LVBIT=H, LVFMT=H)

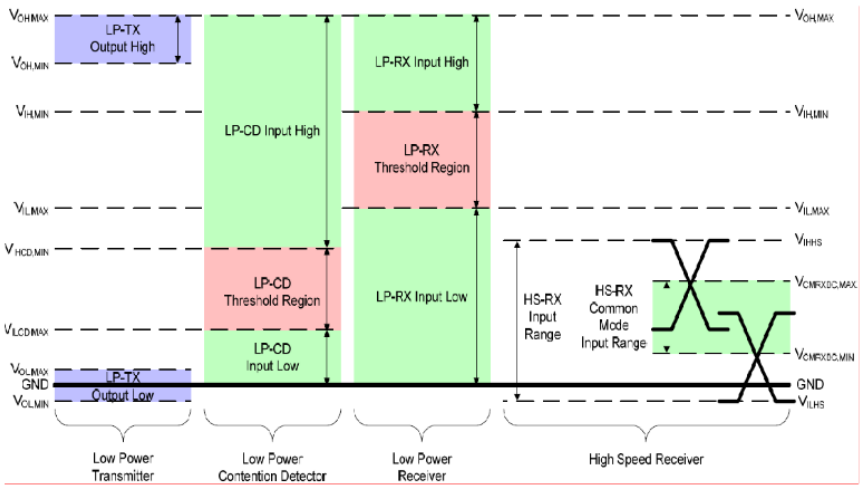
Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-20	-	+70	°C
Storage Temperature Range	T_{ST}	Absolute Max	-30	-	+80	°C
Supply Voltage	V_{DD}	-	2.5	3.3	3.6	V
Supply Current	I_{DD}	V_{DD} = 3.3V	-	55	72	mA
"H" Level input	V_{IH}	-	0.7 * V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	GND	-	0.3* V_{DD}	V
"H" Level output	V_{OH}	-	0.8* V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	GND	-	0.2* V_{DD}	V
Backlight Supply Current	I_{LED}	-	150	170	190	mA
Backlight Supply Voltage	V_{LED}	I_{LED} = 170mA	15.6	18	19.2	V
Backlight Lifetime*	-	T_{OP} = 25°C	30,000	-	-	Hrs.

*Backlight lifetime is rated as Hours until **half-brightness**, under normal operating conditions. The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

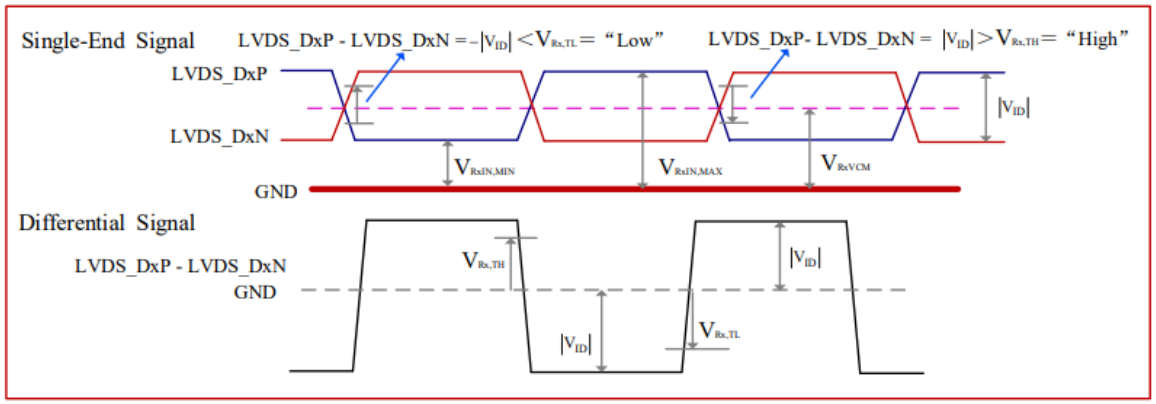
MIPI Characteristics

LPDT Input Characteristics						
Pad Signal Voltge Range	VI	-	-50	-	1350	mV
Ground Shift	VGNDSH	-	-50	-	50	mV
Logic 0 Input Threshold	VIL	-	0	-	550	mV
Logic 1 Input Threshold	VIH	-	880	-	MV1P2	mV
Input Hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output Low Level	VOL	-	-50	-	50	mV
Output High Level	VOH	-	1.1	1.2	1.3	V
Logic 1 Contention Threshold	VILCD, MIN	-	450	-	MV1P2	mV
Logic 0 Contention Threshold	VIHCD, MAX	-	0	-	200	mV
Output Impedance of LPDT	ZOLP	-	80	100	125	ohm
Hi-speed Input/Output Characteristics						
Single-end Input Low Voltage	VILHS	-	-40	-	-	mV
Single-end Input High Voltage	VIHHS	-	-	-	460	mV
Common Mode Voltage	VCMRXDC	-	70	-	330	mV
Hi-speed Transmit Voltage	VOD	-	140	200	250	mV
Differential Input Impedance	ZID	-	80	100	125	ohm



LVDS Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Differential Input High Threshold Voltage	$V_{RX,TH}$	V_{RXVCM}=1.2V	-	-	0.1	V
Differential Input Low Threshold Voltage	$V_{RX,TL}$		-0.1	-	-	V
Input Voltage Range (single-end)	V_{RXIN}		0	-	1.8	V
Differential Input Common Mode Voltage	V_{RXVCM}		|VID|/2	1.2	1.8-|VID|/2	V
Differential Input Voltage	|VID|		0.2	-	0.6	V
Differential Input Leakage Current	I_{LCLVDS}		-10	-	10	uA
Differential Input Impedance	ZID		80	100	140	Ω



Optical Characteristics

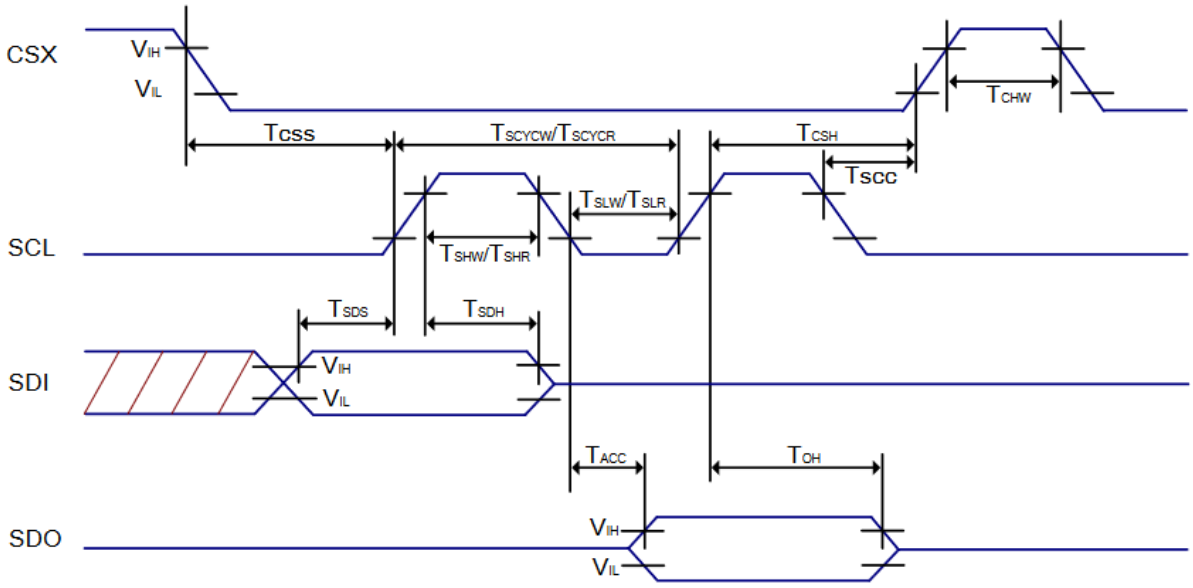
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	ϕY+	-	-	85	-	o
	Bottom	ϕY-		-	85	-	o
	Left	θX-		-	85	-	o
	Right	θX+		-	85	-	o
Contrast Ratio		CR	-	700	1000	-	-
Luminance		L_V	I_{LED} = 170mA	1000	1200	-	cd/m^2
Response Time (Rise + Fall)		$T_R + T_F$	T_{OP} = 25°C	-	30	40	ms
Chromaticity	Red	X_R	-	0.577	0.627	0.677	-
		Y_R	-	0.283	0.333	0.383	-
	Green	X_G	-	0.239	0.289	0.339	-
		Y_G	-	0.522	0.572	0.622	-
	Blue	X_B	-	0.095	0.145	0.195	-
		Y_B	-	0.028	0.058	0.108	-
	White	X_W	-	0.214	0.264	0.314	-
		Y_W	-	0.228	0.278	0.328	-

Driver Information

Built-in NV3051F-L Source Driver: https://support.newhavendisplay.com/hc/en-us/articles/25416096369431-NV3051F-L

Timing Characteristics

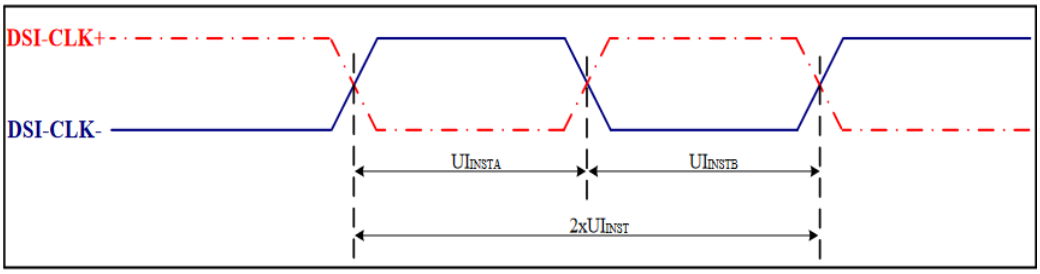
SPI Interface

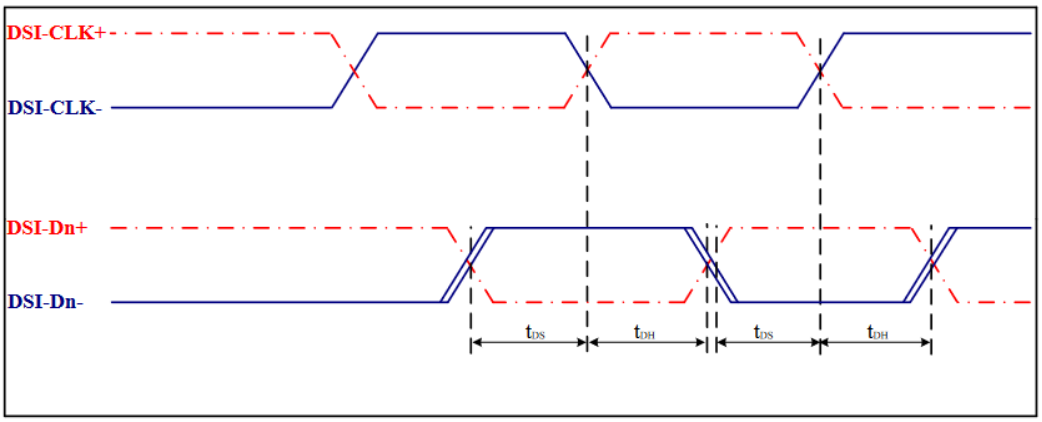


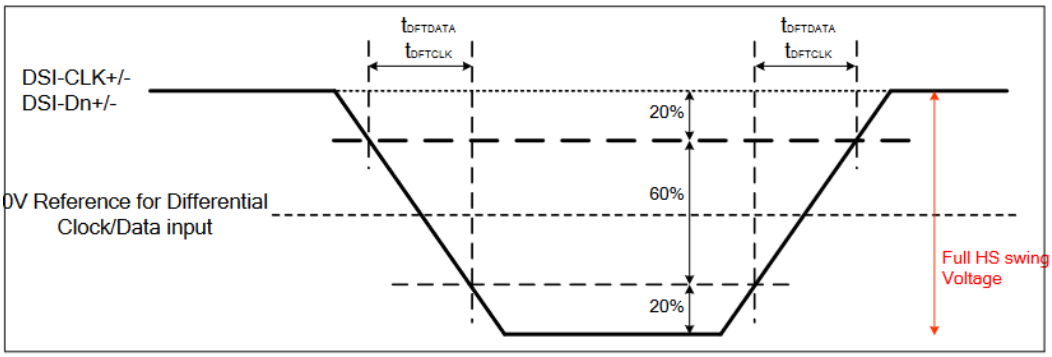
Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	Tcss	Chip select setup time	15	-	ns	-
	TCSH	Chip select hold time	15	-	ns	
	TSCC	Chip select setup time	20	-	ns	
	TCHW	Chip "H" pulse width	40	-	ns	
SCL	TSCYCW	Serial clock cycle (Write)	66	-	ns	-
	TSHW	SCL "H" pulse width (Write)	10	-	ns	
	TSLW	SCL "L" pulse width (Write)	10	-	ns	
	TSCYCR	Serial clock cycle (Read)	150	-	ns	-
	TSHR	SCL"H" pulse width (Read)	60	-	ns	
	TSLR	SCL"L" pulse width (Read)	60	-	ns	
SDI	TSDS	Data setup time	10	-	ns	-
	TSDH	Data hold time	10	-	ns	
	TACC	Access time	10	50	ns	For maximum CL=30pf For minimum CL=8pf
	TOH	Output disable time	15	50	ns	

MIPI DSI Interface

High Speed Mode

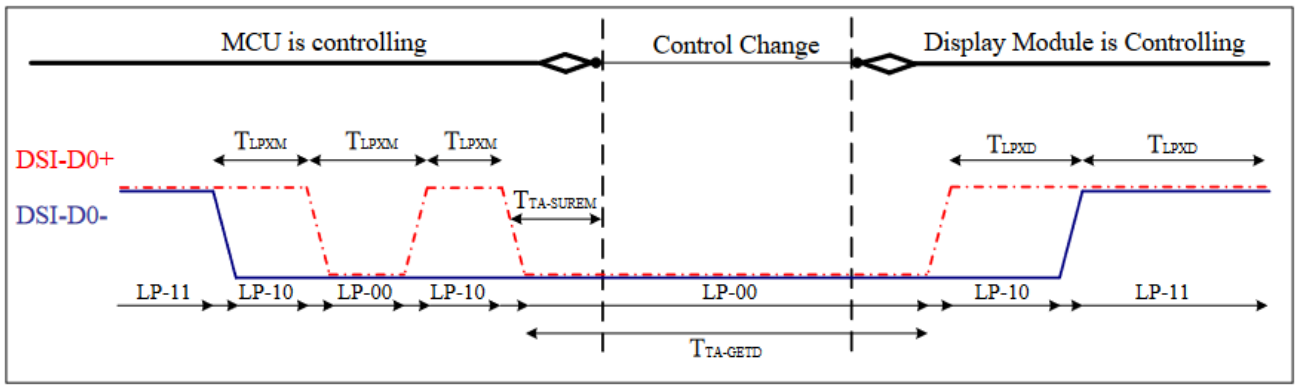


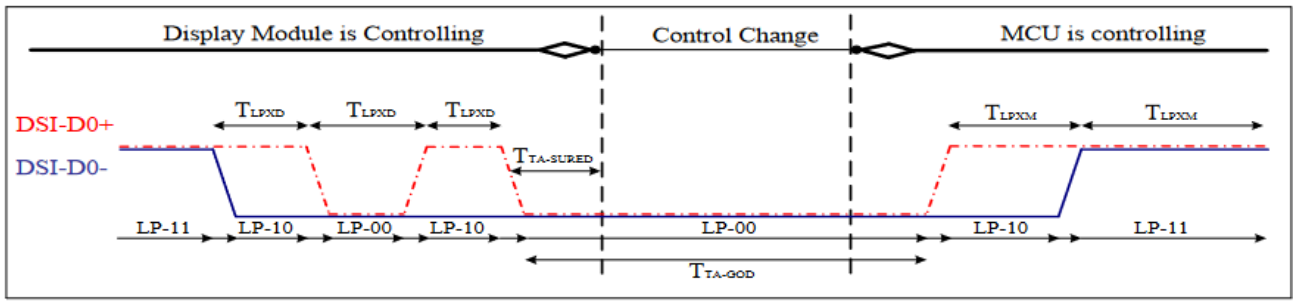




Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2Xui_{inst}$	Double UI instantaneous	2.22	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	1.11	-	12.5	ns
DSI-Dn+/-	T_{ds}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	T_{dh}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	T_{drtclk}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{drtdata}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	T_{dftclk}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$T_{dftdata}$	Differential fall time for data	150	-	0.3UI	ps

Low Power Mode





Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						
DSI-D0+/-	TLPXM	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	-	ns
DSI- D0+/-	TLPXD	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Modulen MPU	58	-	-	ns
DSI- D0+/-	TTA-SURED	Time-out before the MPU start driving	TLPXD	-	2XTLPXD	ns
DSI- D0+/-	TTA-GETD	Time to drive LP-00 by display module	5XTLPXD	-	-	ns
DSI- D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request – MPU	4XTLPXD	-	-	ns
DSI- D0+/-	Ratio TLPX	Ratio of TLPXM / TLPXD between MCU and display module	2/3	-	3/2	

Bursts

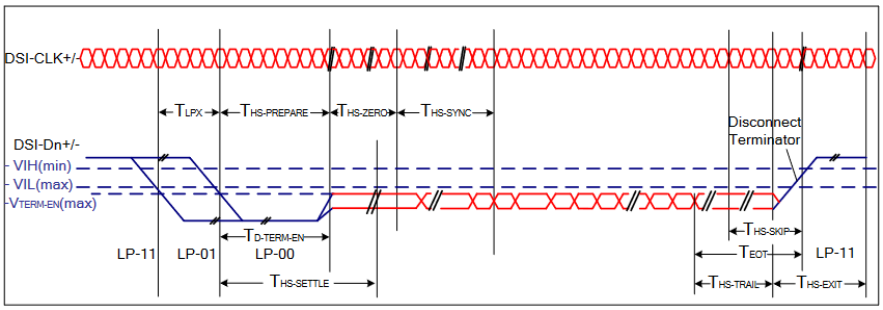


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	TLPX	Length of any low-power state period	50	-	-	ns
DSI- Dn+/-	THS- PREPARE	Time to drive LP-00 to prepare for HS transmission	40ns+4UI	-	85ns+6UI	ns
DSI- Dn+/-	THS-PREPARE+THS-ZERO	THS-PREPARE+time to drive HS-0 before the sync sequence	145ns+10UI	-	-	ns
DSI- Dn+/-	TD-TERM- EN	Time to enable Data Lane receiver line termination measured from when Dn crosses VIL(max)	Time for Dn to reach VTERM-EN	-	35ns+4UI	ns
DSI- Dn+/-	THS-SKIP	Time-out at RX to ignore transition period of EoT	40	-	55ns+4UI	ns
DSI- Dn+/-	THS-TRAIL	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI- Dn+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	-	ns
DSI- Dn+/-	TeoT	Time from start of THS-TRAIL period to start of LP-11 state	-	-	105ns+12UI	ns

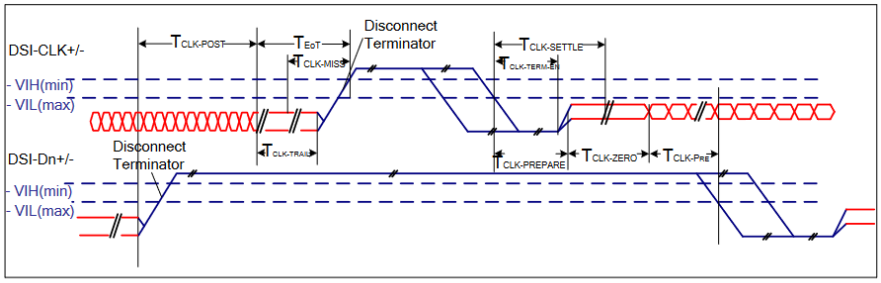
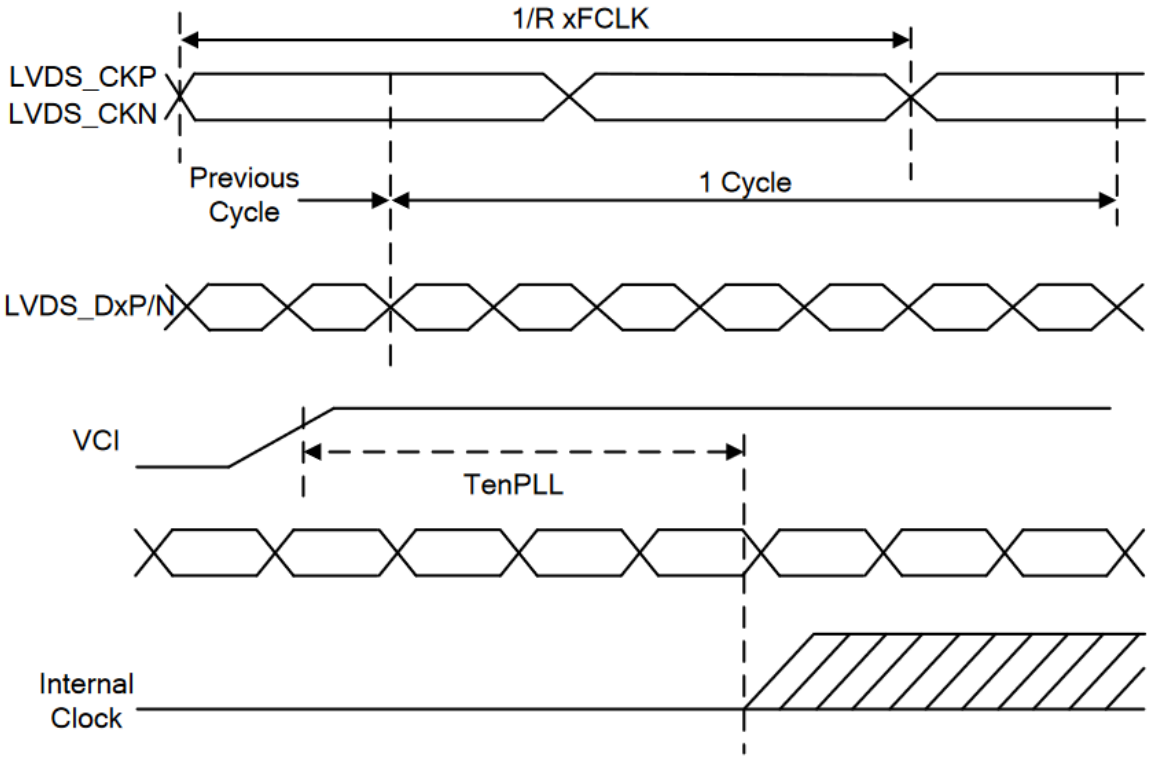


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	TCLK-POST	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns+52UI	-	-	ns
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS clock transmission	38	-	95	ns
DSI-CLK+/-	TCLK-TERM- EN	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach VTERM-EN	-	38	ns
DSI- CLK+/-	TCLK-PREPARE +TCLK-ZERO	TCLK-PREPARE + time for lead HS-0 drive period before starting Clock	300	-	-	ns
DSI- CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	TeoT	Time from start of TCLK-TRAIL period to start of LP-11 state	-	-	105ns+ 12UI	ns

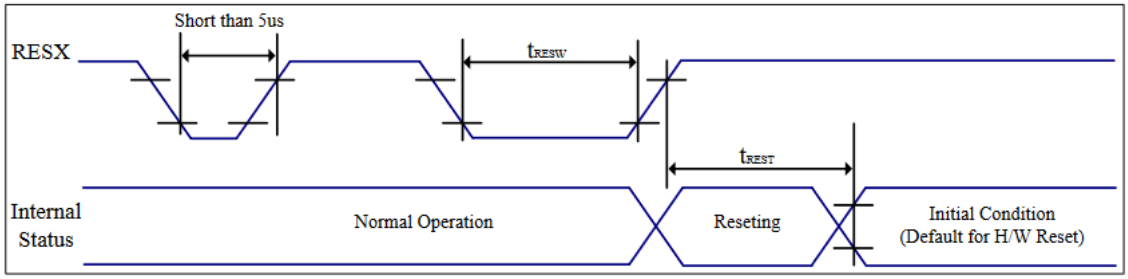
LVDS Interface

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	RxFCLK	-	30	-	71	MHz
Input data skew margin	TRSKM	|VID|=200mV RxVCM=1.2V RxFCLK=71MHz	500	-	-	ps
Clock High Time	TLVCH	-	-	4/(7*RxFCLK)	-	ns
Clock Low Time	TLVCL	-	-	3/(7*RxFCLK)	-	ns
PLL wake-up-time	TenPLL	-	-	-	150	us



Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Modulation Frequency	SSC_{MF}	23	-	93	KHz	
Modulation Rate	SSC_{MR}	-	-	+3	%	

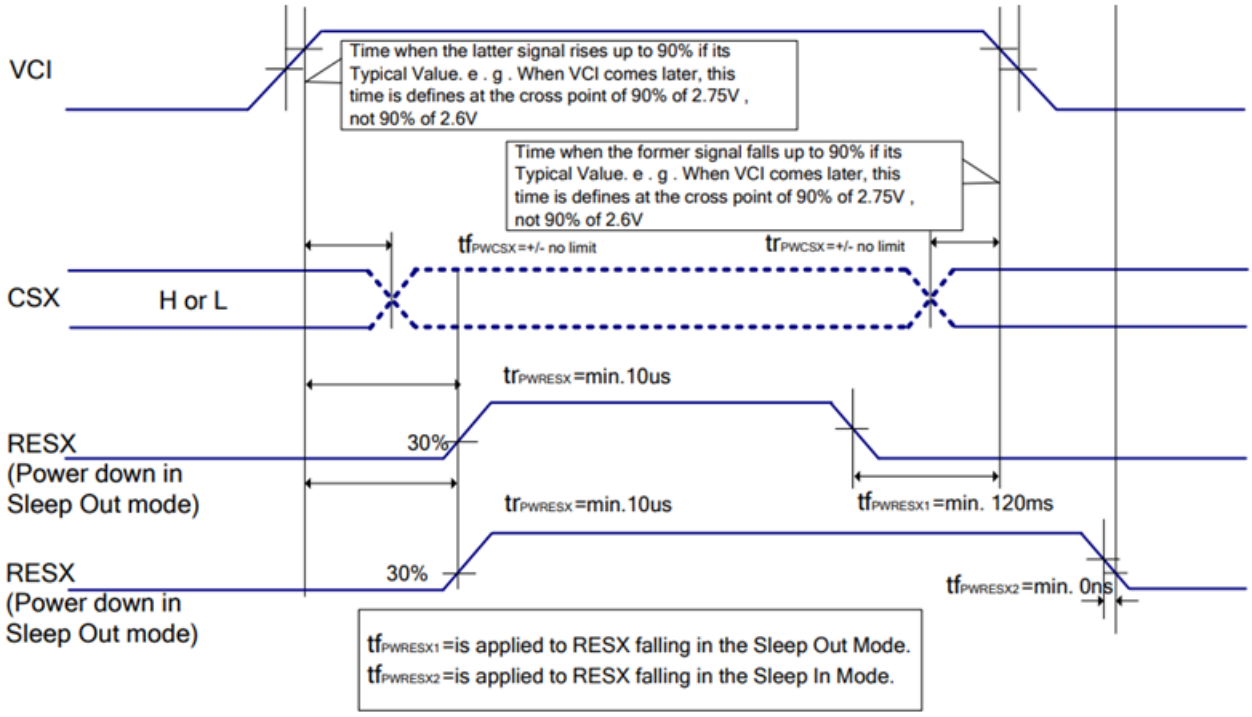
Reset Timing



Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
T_{resw}	*1) Reset low pulse width	RESX	10	-	-	-	us
T_{rest}	*2) Reset complete time	-	-	-	5	When reset applied during Sleep in mode	ms
		-	-	-	120	When reset applied during Sleep out mode	ms

Power ON/OFF Sequence

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10us after VCI has been applied



Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C 240hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 240hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C , 90% RH , 240hrs	1,2
Thermal Shock resistance	Endurance test applying the high thermal with high humidity stress for a long time.	-30°C ← 25°C →+80°C (30 min ← 3 min → 30min) 100 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	Frequency range:10Hz~50Hz Acceleration of gravity:5G X, Y, Z 30 min for each direction	3
Static electricity test	Endurance test applying electric static discharge.	Air: ±8kV 150pF/330Ω ; Contact: ±4kV 150pF/330Ω For 10 times each.	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.