NEWHAVEN DISPLAY INTERNATIONAL

Product Specification

NHD-4.0-480480AF-MSXP

TFT Liquid Crystal Display

NHD-	Newhaven Display
4.0-	4.0" Diagonal
480480-	480xRGBx480 Pixels
AF-	Model
M-	MIPI Interface
S-	White LED Backlight
X-	TFT
P-	IPS, Wide Temperature

Newhaven Display International, Inc.
2661 Galvin Court, Elgin, IL 60124 USA

Ph: 847.844.8795 | Fx: 847.844.8796
www.newhavendisplay.com

REACH Compliant

RoHS Compliant

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Additional Resources

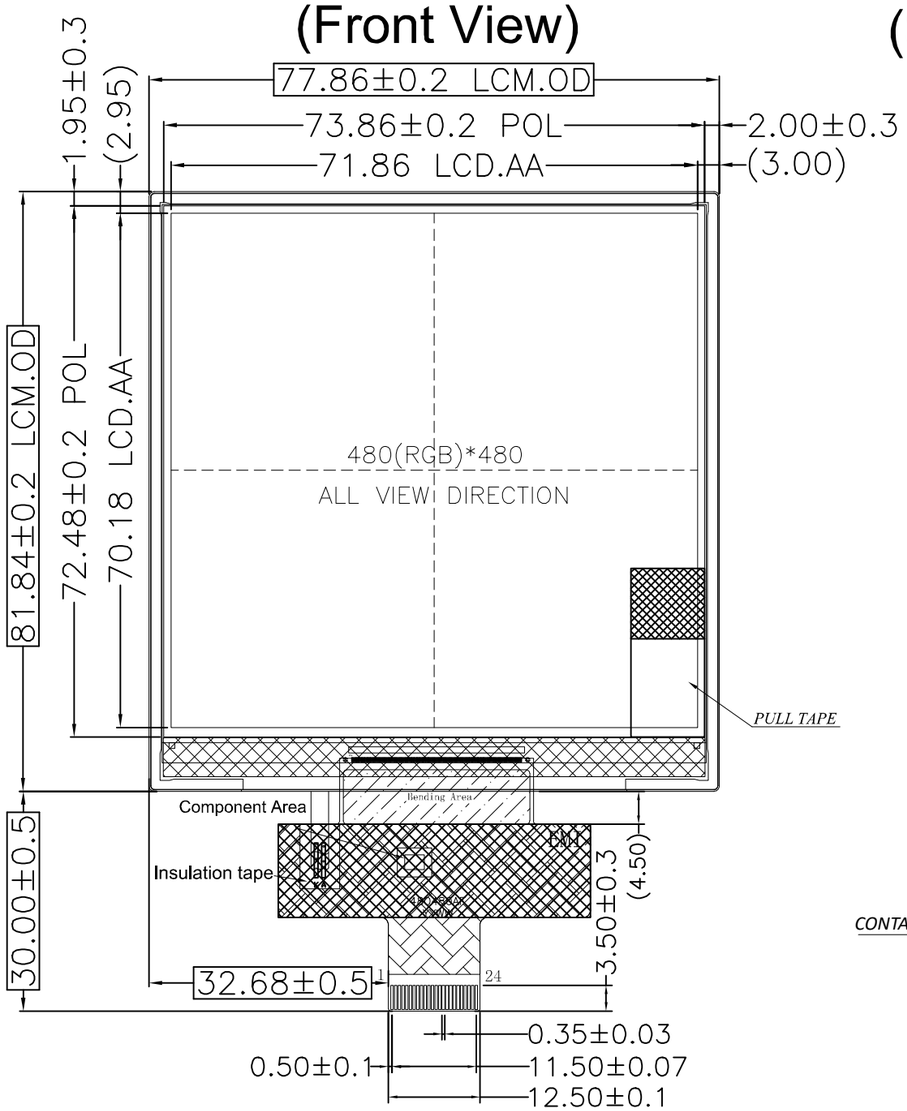
- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

Document Revision History

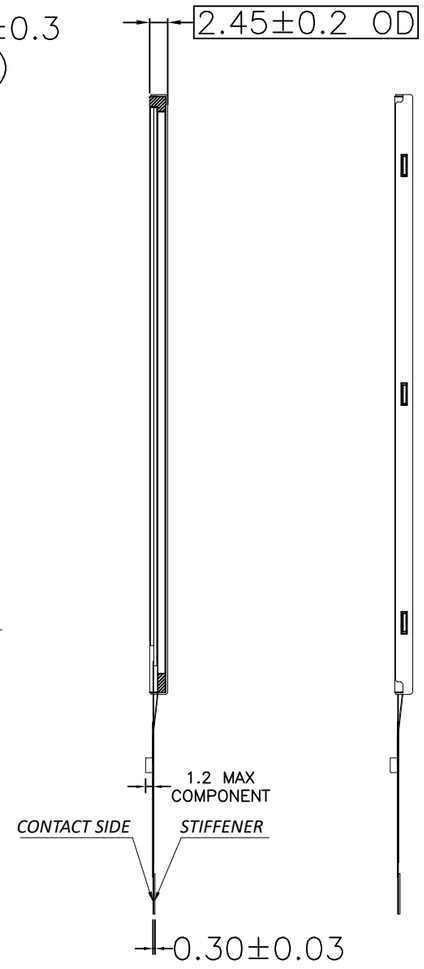
Revision	Date	Description	Changed By
-	09/15/2025	Initial Release	KL
1	02/18/2026	Recommended Connector Information Updated	KL

Mechanical Drawing

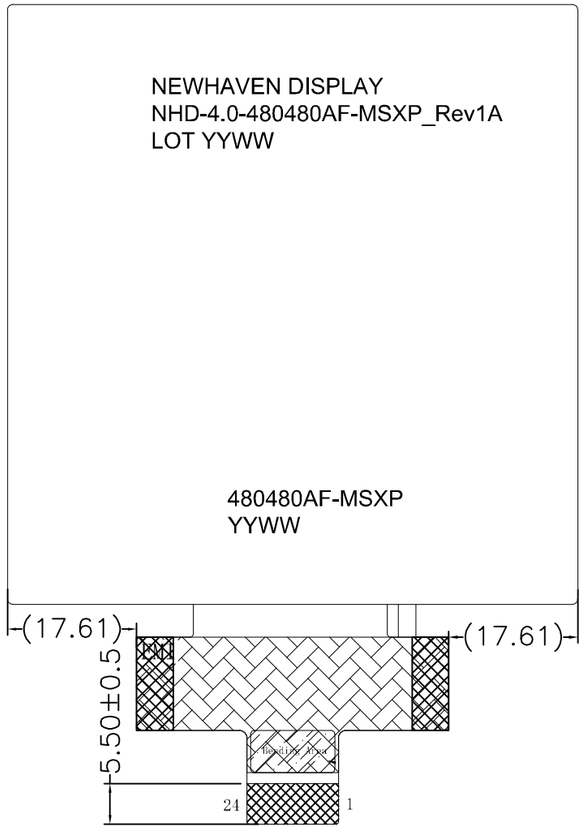
(Front View)



(Side View)



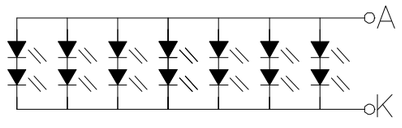
(Back View)



1	LED_K
2	LED_A
3	NC
4	VDD
5	GND
6	DN0
7	DP0
8	GND
9	CN
10	CP
11	GND
12	DN1
13	DP1
14	GND
15	RESETX
16	CSX
17	SCL
18	SDA
19	SDO
20	TE_L
21	IM0
22	IM1
23	IM3
24	LANSEL

Product Description: 4.0” 480x480 IPS TFT

1. Driver IC: ST7701SN
2. Interface: 2-lane MIPI DSI
3. Power Requirement: 3.3V TFT, 6.1V/140mA Backlight
4. Optical Features: Normally Black, Transmissive, Anti-Glare, 1000cd/m²
5. Recommended FFC Connector: 24pin 0.5mm pitch; Ex. Molex 524352471
6. Built-in EMI Shielding



CIRCUIT DIAGRAM

Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

Drawing/Part Number: NHD-4.0-480480AF-MSXP
Revision: 1A

Unless otherwise specified:
• Dimensions are in Millimeters
• Third Angle Projection

Drawn By: K. Lewis
Drawn Date: 02/18/2026
Approved By: K. Lewis
Approved Date: 02/18/2026

Pin Description

Pin No.	Symbol	External Connection	Function Description
1	LED_K	Power Supply	Backlight Cathode (Ground)
2	LED_A	Power Supply	Backlight Anode (140mA @ 6.1V)
3	NC	-	No Connect
4	VDD	Power Supply	Supply Voltage for LCD and Logic (3.3V)
5	GND	Power Supply	Ground
6	DN0	MPU	MIPI DSI Differential Data signal
7	DP0	MPU	MIPI DSI Differential Data signal
8	GND	Power Supply	Ground
9	CN	MPU	MIPI DSI Differential clock signal
10	CP	MPU	MIPI DSI Differential clock signal
11	GND	Power Supply	Ground
12	DN1	MPU	MIPI DSI Differential Data signal
13	DP1	MPU	MIPI DSI Differential Data signal
14	GND	Power Supply	Ground
15	RESETX	MPU	Active LOW Reset signal
16	CSX	MPU	Active LOW Chip Select signal
17	SCL	MPU	Serial Clock signal for SPI interface
18	SDA	MPU	Serial Data Input signal for SPI interface
19	SD0	MPU	Serial Data Output signal for SPI interface
20	TE_L	MPU	Tearing Effect Output signal (active low)
21	IM0	MPU	Interface Mode Selection
22	IM1	MPU	Interface Mode Selection
23	IM3	MPU	Interface Mode Selection
24	LANSEL	MPU	Interface Mode Selection

Recommended LCD connector: 24pin 0.5mm pitch FFC; Ex. Molex 524352471

Interface Selection

Pin Name	MIPI DSI	MIPI + 16b_SPI (fall)	MIPI + 16b_SPI (Rise)
IM0	1	0	0
IM1	0	1	1
IM3	0/1	1	0

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-20	-	+70	°C
Storage Temperature Range	T_{ST}	Absolute Max	-30	-	+80	°C
Supply Voltage	V_{DD}	-	2.5	3.3	3.6	V
Supply Current	I_{DD}	V_{DD} = 3.3V	-	43	65	mA
"H" Level input	V_{IH}	-	0.7*V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	V_{SS}	-	0.3*V_{DD}	V
"H" Level output	V_{OH}	-	0.8*V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	V_{SS}	-	0.2*V_{DD}	V
Backlight Supply Current	I_{LED}	-	117	140	168	mA
Backlight Supply Voltage	V_{LED}	I_{LED} = 140mA T_{OP} = 25°C	5.4	6.1	6.8	V
Backlight Lifetime*	-		30,000	-	-	Hrs.

*Backlight lifetime is rated as Hours until **half-brightness**, under normal operating conditions. The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	ϕY+	CR ≥ 10	-	80	-	°
	Bottom	ϕY-		-	80	-	°
	Left	θX-		-	80	-	°
	Right	θX+		-	80	-	°
Contrast Ratio		CR	-	640	800	-	-
Luminance		L_V	I_{LED} =140mA	700	1000	1500	cd/m²
Response Time (Rise + Fall)		$T_R + T_F$	T_{OP} = 25°C	-	25	35	ms
Chromaticity	Red	X_R	-	0.58	0.61	0.64	-
		Y_R	-	0.32	0.35	0.38	-
	Green	X_G	-	0.27	0.30	0.33	-
		Y_G	-	0.57	0.60	0.63	-
	Blue	X_B	-	0.11	0.14	0.17	-
		Y_B	-	0.05	0.08	0.11	-
	White	X_W	-	0.25	0.28	0.31	-
		Y_W	-	0.28	0.31	0.34	-

Driver Information

Built-in ST7701SN Driver: https://support.newhavendisplay.com/hc/en-us/articles/14147699906711-ST7701SN

Recommended Timing Values

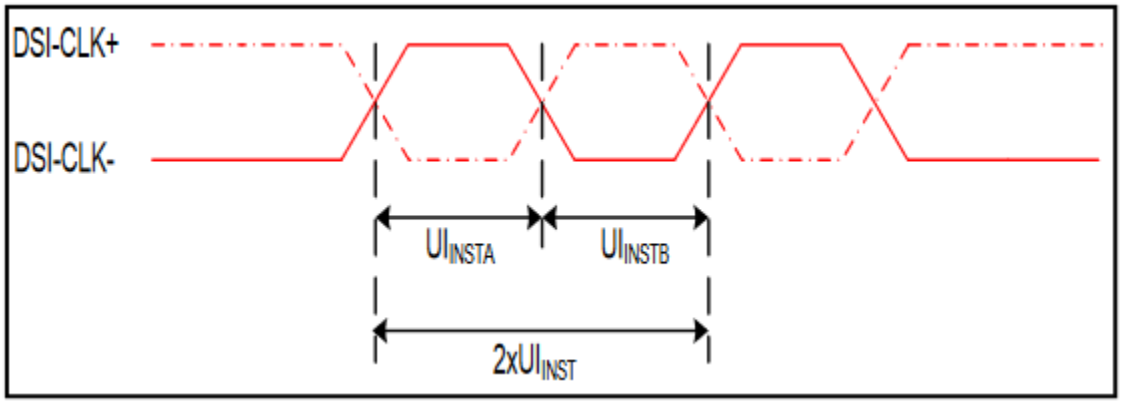
Recommended MIPI Timing Values:

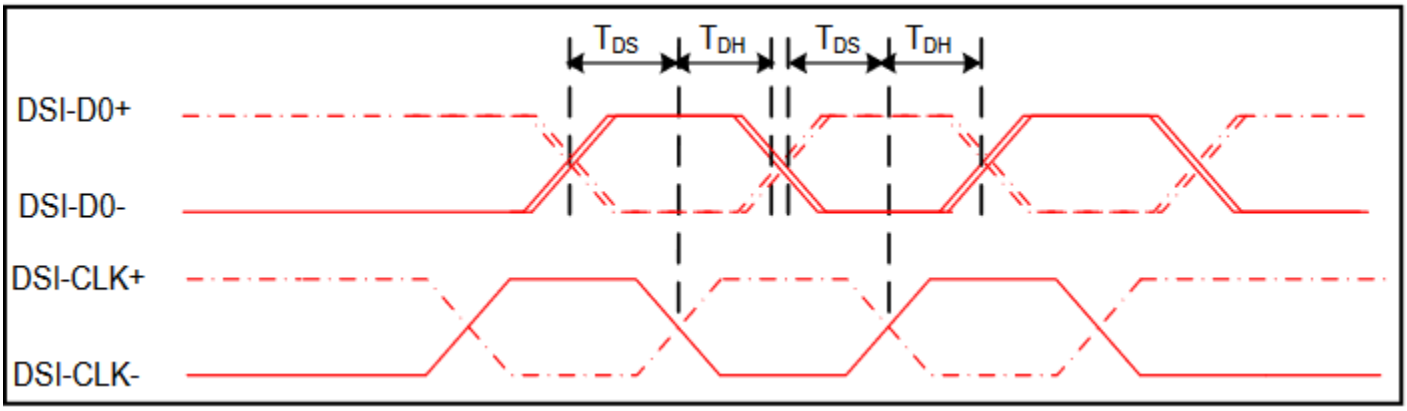
HS Total	HFP	HBP	HS Pulse	VS Total	VFP	VBP	VS Pulse	PCLK Freq
790	150	150	10	530	20	20	10	25 MHz

Timing Characteristics

MIPI DSI Interface Characteristics

High Speed Mode





DSI timing characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	2.5	25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs	1.25	12.5	ns	UI = UI_{INSTA}= UI_{INSTB}
DSI-Dn+/-	tDS	Data to clock setup time	0.15	-	UI	
DSI-Dn+/-	tDH	Data to clock hold time	0.15	-	UI	

Table 7 Mipi Interface- High Speed Mode Timing Characteristics

Low Power Mode

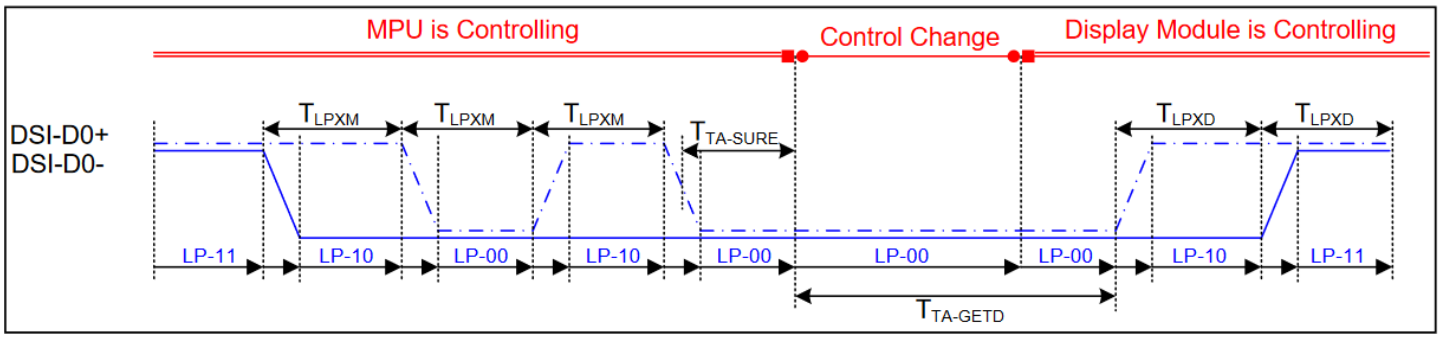


Figure 6 Bus Turnaround (BTA) from display module to MPU Timing

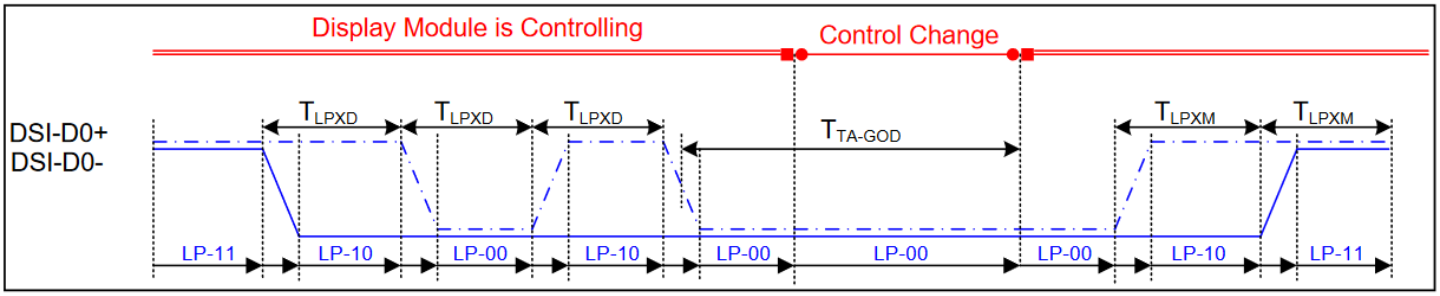


Figure 7 Bus Turnaround (BTA) from MPU to display module Timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
DSI-D0+/-	TLPXM	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Input
DSI-D0+/-	TLPXD	Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module	50	75	ns	Output
DSI-D0+/-	TTA-SURED	Time-out before the MPU start driving	T_{LPXD}	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	TTA-GETD	Time to drive LP-00 by display module	$5xT_{LPXD}$		ns	Input
DSI-D0+/-	TTA-GOD	Time to drive LP-00 after turnaround request-MPU	$4xT_{LPXD}$		ns	Output

Table 8 Mipi Interface Low Power Mode Timing Characteristics

DSI Burst Mode

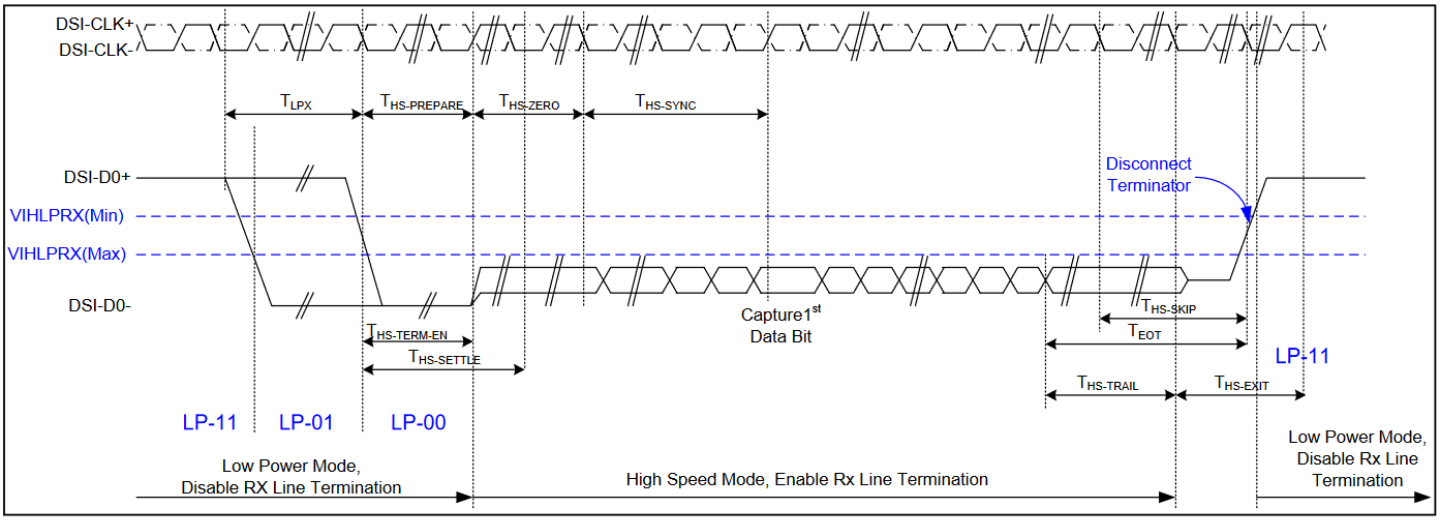


Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing						
DSI-Dn+/-	TLPX	Length of any low power state period	50	-	ns	Input
DSI-Dn+/-	THS-PREPARE	Time to drive LP-00 to prepare for HS transmission	40+4 UI	85+6 UI	ns	Input
DSI-Dn+/-	THS-TERM-EN	Time to enable data receiver line termination measured from when Dn crosses VILMAX	-	35+4 UI	ns	Input
DSI-Dn+/-	THS-PREPARE + THS-ZERO	THS-PREPARE + time to drive HS-0 before the sync sequence	140+ 10UI	-	ns	Input

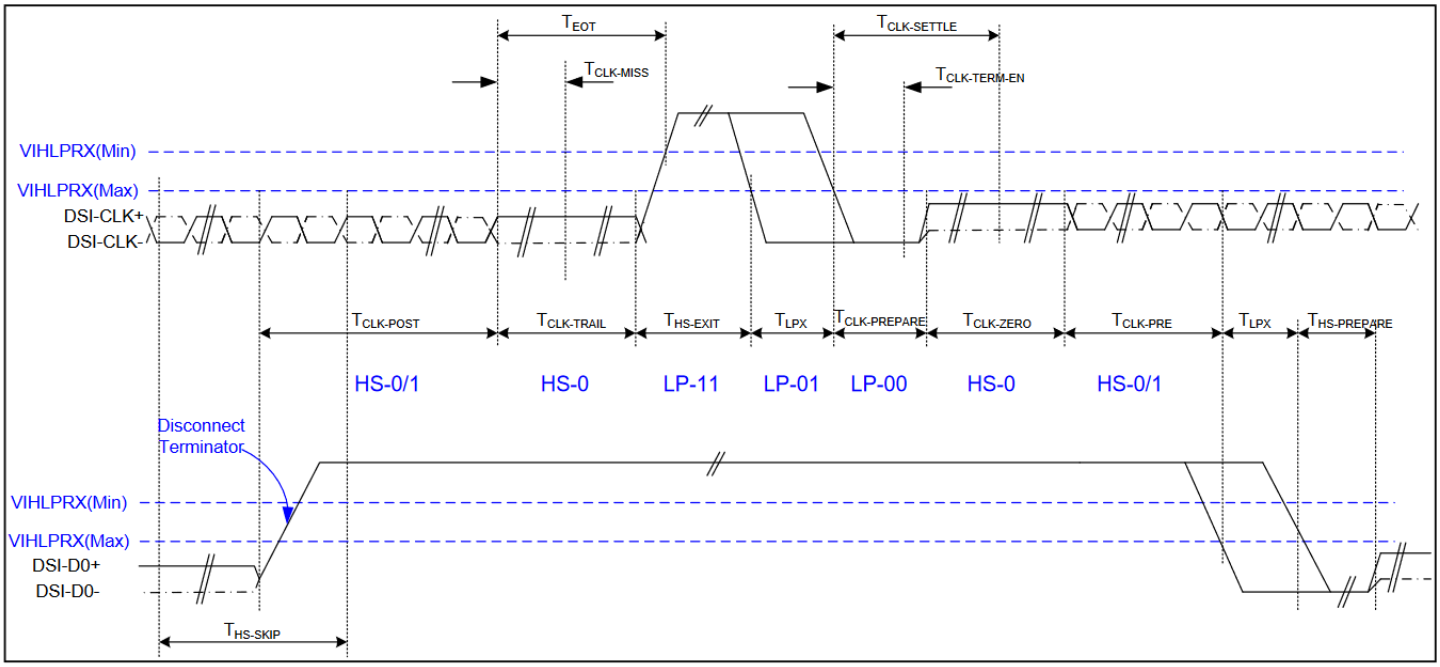
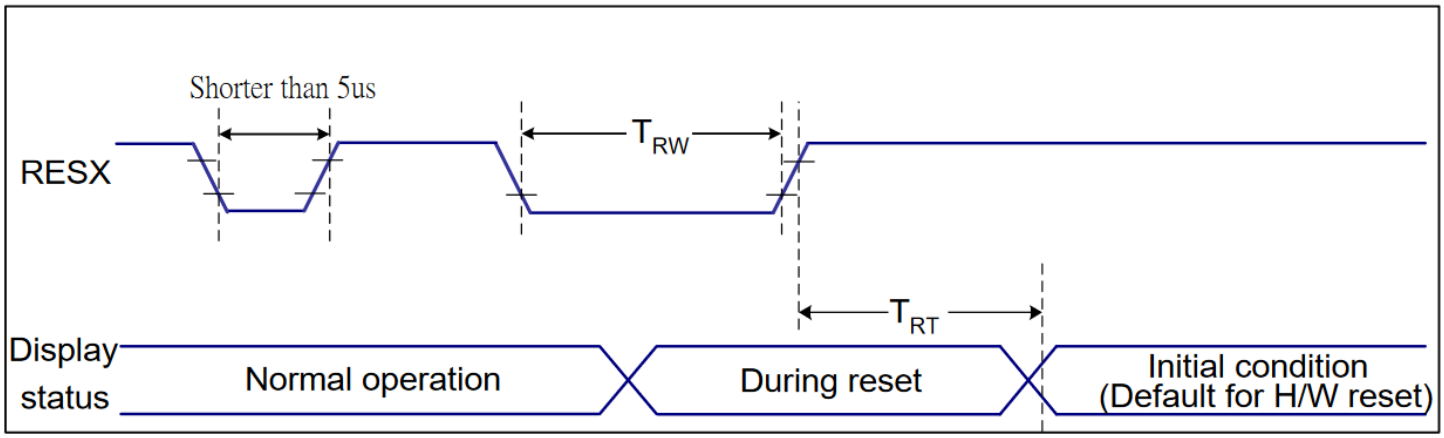


Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing

High Speed Mode to/from Low Power Mode Timing						
DSI-CLK+/-	TCLK-POS	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+5 2UI	-	ns	Input
DSI-CLK+/-	TCLK-TRAIL	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns	Input
DSI-CLK+/-	THS-EXIT	Time to drive LP-11 after HS burst	100	-	ns	Input
DSI-CLK+/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38	95	ns	Input
DSI-CLK+/-	TCLK-TERM-EN	Time-out at clock lan display module to enable HS transmission	--	38	ns	Input
DSI-CLK+/-	TCLK-PREPARE + TCLK-ZERO	Minimum lead HS-0 drive period before starting clock	300	-	ns	Input
DSI-CLK+/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8UI	-	ns	Input
DSI-CLK+/-	TEOT	Time form start of TCLK-TRAIL period to start of LP-11 state	-	105n s+12 UI	ns	Input

Reset Input Timing



Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120(Note 1, 6, 7)	ms

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 240hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 240hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C , 120hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 120hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+50°C , 90% RH , 120hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-30°C,30min -> 25°C,10min -> 80°C,30min 10 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	Frequency range:250r/min Amplitude: 1 inch Time: 45min	3
Static electricity test	Endurance test applying electric static discharge.	Air: Vs=±8kV 10 Times	
		Contact: Vs= ±4kV 10 Times	

Note 1: No condensation to be observed.
Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.