NEWHAVEN DISPLAY INTERNATIONAL

**Product Specification**

# NHD-2.1-480480AF-ASXP

## TFT Liquid Crystal Display

| | |
|---|---|
| **NHD-** | Newhaven Display |
| **2.1-** | 2.1" Diagonal |
| **480480-** | 480xRGBx480 Pixels |
| **AF-** | Model |
| **A-** | Built-in Driver / No Controller |
| **S-** | High Brightness, White LED Backlight |
| **X-** | TFT |
| **P-** | IPS, Wide Temperature |

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REACH Compliant

RoHS Compliant

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# Table of Contents



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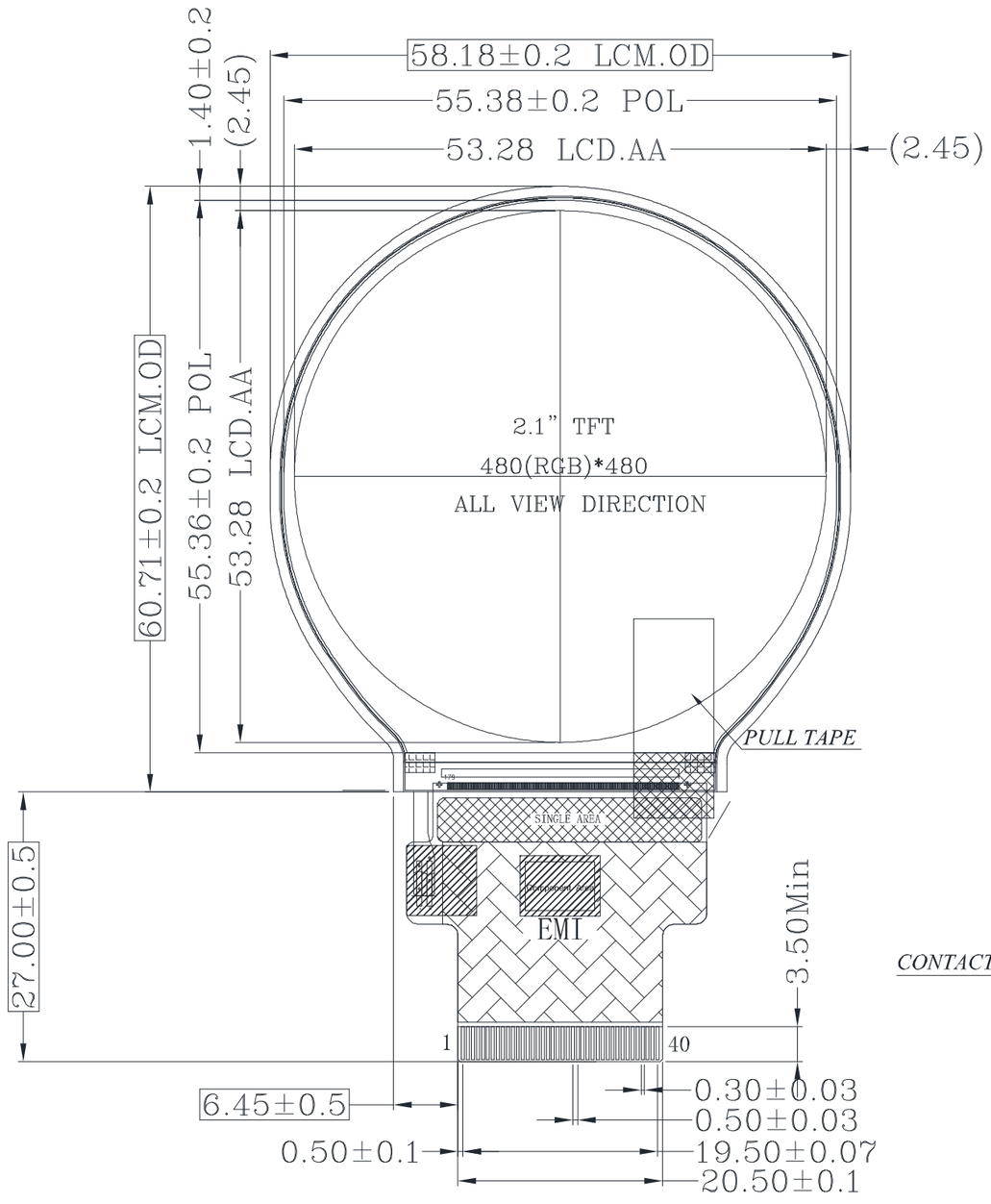
## Additional Resources

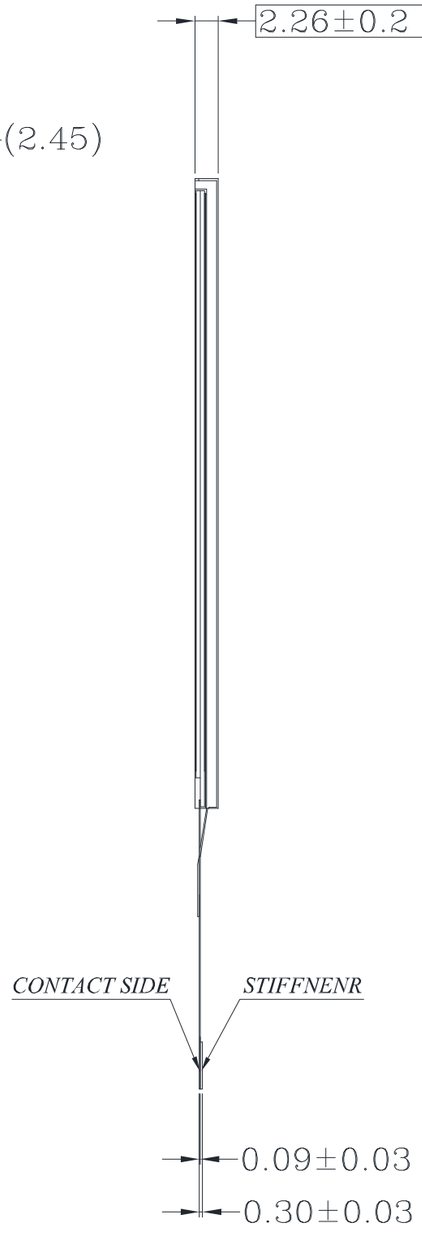
- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

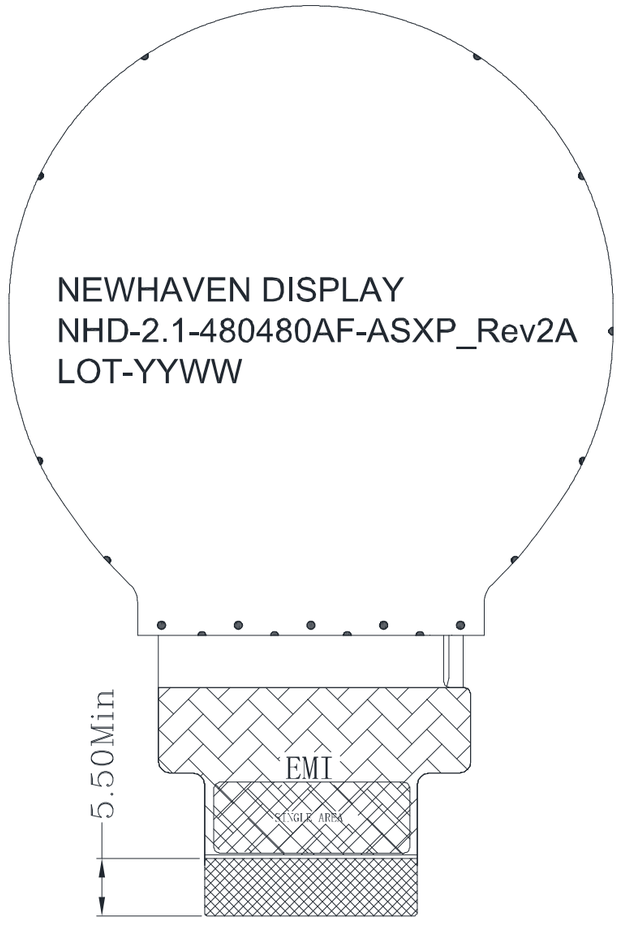
# Document Revision History

| Revision | Date | Description | Changed By |
|---|---|---|---|
| - | 07/01/2024 | Initial Release | KL |

# Mechanical Drawing



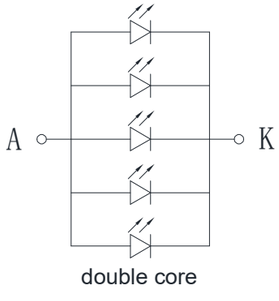




| PIN | SYMBOL |
|---|---|
| 1 | LED_K |
| 2 | LED_A |
| 3 | VDD |
| 4 | GND |
| 5 | DN0 |
| 6 | DP0 |
| 7 | GND |
| 8 | CN |
| 9 | CP |
| 10 | GND |
| 11 | VS |
| 12 | HS |
| 13 | PCLK |
| 14 | DE |
| 15 | DB0(B0) |
| 16 | DB1(B1) |
| 17 | DB2(B2) |
| 18 | DB3(B3) |
| 19 | DB4(B4) |
| 20 | DB5(B5) |
| 21 | DB8(G0) |
| 22 | DB9(G1) |
| 23 | DB10(G2) |
| 24 | DB11(G3) |
| 25 | DB12(G4) |
| 26 | DB13(G5) |
| 27 | DB16(R0) |
| 28 | DB17(R1) |
| 29 | DB18(R2) |
| 30 | DB19(R3) |
| 31 | DB20(R4) |
| 32 | DB21(R5) |
| 33 | RESETX |
| 34 | CSX |
| 35 | SCL |
| 36 | DCX |
| 37 | SDA |
| 38 | IM0 |
| 39 | IM1 |
| 40 | IM2 |

Product Description: 2.1" 480x480 IPS TFT

1. Driver IC: ST7701S
2. Interface: 18-bit Parallel RGB, 1-lane MIPI DSI
3. Power Requirement: 3.3V TFT, 6.0V/100mA Backlight
4. Optical Features: Normally Black, Transmissive, Anti-Glare, 1000cd/m²
5. Recommended FFC Connector: 40pin 0.5mm pitch; Ex. Molex 54104-4096
6. EMI Shielded FPC




**Standard Tolerance:**
(Unless otherwise specified)
Linear: ±0.3mm

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| | | |
|---|---|---|
| Drawing/Part Number: NHD-2.1-480480AF-ASXP | | Revision: 2A |
| **Unless otherwise specified:** • Dimensions are in Millimeters • Third Angle Projection | Drawn By: K. Lewis | Approved By: K.. Lewis |
| | Drawn Date: 04/24/2024 | Approved Date: 04/24/2024 |

# Pin Description

| Pin No. | Symbol | External Connection | Function Description |
|---|---|---|---|
| 1 | LED_K | Power Supply | Backlight Cathode (Ground) |
| 2 | LED_A | Power Supply | Backlight Anode (100mA @ 6V) |
| 3 | VDD | Power Supply | Supply Voltage for LCD and Logic (3.3V) |
| 4 | GND | Power Supply | Ground |
| 5 | DN0 | MPU | MIPI DSI Differential Data signal |
| 6 | DP0 | MPU | MIPI DSI Differential Data signal |
| 7 | GND | Power Supply | Ground |
| 8 | CN | MPU | MIPI DSI Differential Clock signal |
| 9 | CP | MPU | MIPI DSI Differential Clock signal |
| 10 | GND | Power Supply | Ground |
| 11 | VS | MPU | Frame Synchronizing signal for RGB interface |
| 12 | HS | MPU | Line Synchronizing signal for RGB interface |
| 13 | PCLK | MPU | Dot Clock signal for RGB interface |
| 14 | DE | MPU | Data Enable signal for RGB interface |
| 15-20 | B0-B5 | MPU | Blue Data signals |
| 21-26 | G0-G5 | MPU | Green Data signals |
| 27-32 | R0-R5 | MPU | Red Data signals |
| 33 | RESETX | MPU | Active LOW Reset signal |
| 34 | CSX | MPU | Active LOW Chip Select signal |
| 35 | SCL | MPU | Serial Clock signal for SPI interface (rising edge) |
| 36 | DCX | MPU | Data/Command selection for SPI: '1' = Data; '0' = Command |
| 37 | SDA | MPU | Serial Data Input signal for SPI interface |
| 38 | IM0 | MPU | Interface Mode Select signal |
| 39 | IM1 | MPU | Interface Mode Select signal |
| 40 | IM2 | MPU | Interface Mode Select signal |

**Recommended LCD connector:** 40pin 0.5mm pitch FFC; Ex. Molex 54104-4031

# Interface Selection

| Pin Name | RGB + 8b_SPI (rise) | RGB + 9b_SPI (rise) | RGB + 16b_SPI (fall) | MIPI DSI | MIPI + 16b_SPI (fall) |
|---|---|---|---|---|---|
| IM0 | 1 | 0 | 1 | 1 | 0 |
| IM1 | 0 | 1 | 1 | 0 | 1 |
| IM2 | 0 | 0 | 0 | 1 | 1 |

IM3 (not shown) is pulled 'high' internally.

# Electrical Characteristics

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Operating Temperature Range | $T_{OP}$ | Absolute Max | -20 | - | +70 | °C |
| Storage Temperature Range | $T_{ST}$ | Absolute Max | -30 | - | +80 | °C |
| Supply Voltage | $V_{DD}$ | - | 2.5 | 3.3 | 3.6 | V |
| Supply Current | $I_{DD}$ | $V_{DD}$ = 3.3V | 12 | 24 | 36 | mA |
| "H" Level input | $V_{IH}$ | - | 0.7*$V_{DD}$ | - | $V_{DD}$ | V |
| "L" Level input | $V_{IL}$ | - | $V_{SS}$ | - | 0.3*$V_{DD}$ | V |
| "H" Level output | $V_{OH}$ | - | 0.8*$V_{DD}$ | - | $V_{DD}$ | V |
| "L" Level output | $V_{OL}$ | - | $V_{SS}$ | - | 0.2*$V_{DD}$ | V |
| | | | | | | |
| Backlight Supply Current | $I_{LED}$ | - | 75 | 100 | 125 | mA |
| Backlight Supply Voltage | $V_{LED}$ | $I_{LED}$ = 100mA<br>$T_{OP}$ = 25°C | 5.5 | 6.0 | 6.5 | V |
| Backlight Lifetime* | - | | 30,000 | - | - | Hrs. |

*Backlight lifetime is rated as Hours until **half-brightness**, under normal operating conditions. The LED of the backlight is driven by current drain; drive voltage is for reference only. Drive voltage must be selected to ensure backlight current drain is below MAX level stated.

# Optical Characteristics:

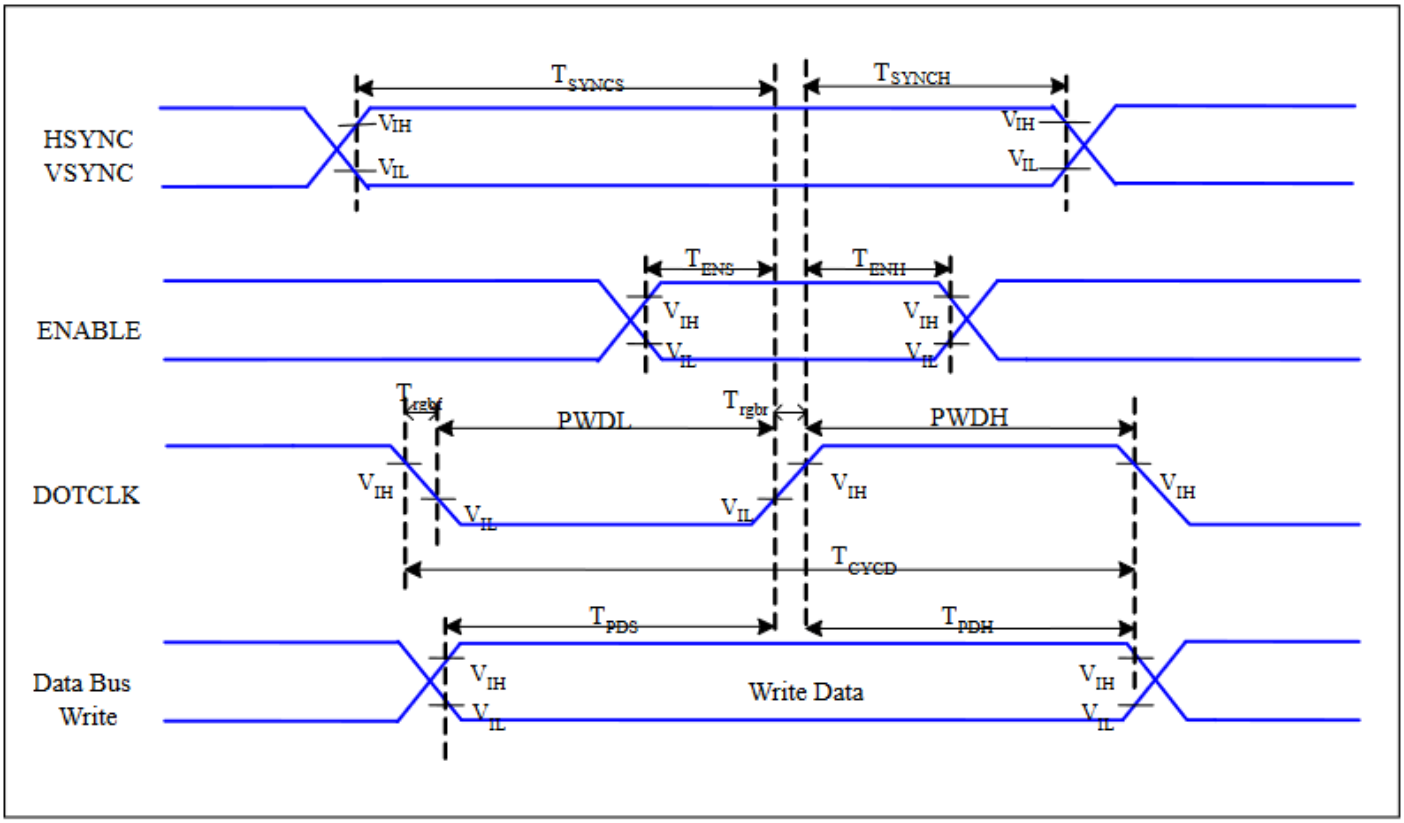
| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Optimal Viewing Angles | Top | φY+ | CR ≥ 10 | - | 85 | - | ° |
| | Bottom | φY- | | - | 85 | - | ° |
| | Left | θX- | | - | 85 | - | ° |
| | Right | θX+ | | - | 85 | - | ° |
| Contrast Ratio | | CR | - | 800 | 1000 | - | - |
| Luminance | | $L_V$ | $I_{LED}$ =100mA | 800 | 1000 | - | cd/m² |
| Response Time (Rise + Fall) | | $T_R + T_F$ | $T_{OP}$ = 25°C | - | 30 | 35 | ms |
| Chromaticity | Red | $X_R$ | - | 0.614 | 0.664 | 0.714 | - |
| | | $Y_R$ | - | 0.263 | 0.313 | 0.363 | - |
| | Green | $X_G$ | - | 0.281 | 0.331 | 0.381 | - |
| | | $Y_G$ | - | 0.574 | 0.624 | 0.674 | - |
| | Blue | $X_B$ | - | 0.068 | 0.118 | 0.168 | - |
| | | $Y_B$ | - | 0.013 | 0.037 | 0.087 | - |
| | White | $X_W$ | - | 0.237 | 0.287 | 0.337 | - |
| | | $Y_W$ | - | 0.254 | 0.304 | 0.350 | - |

# Driver Information

Built-in ST7701S Driver: https://support.newhavendisplay.com/hc/en-us/articles/14549586395031-ST7701S

# Timing Characteristics

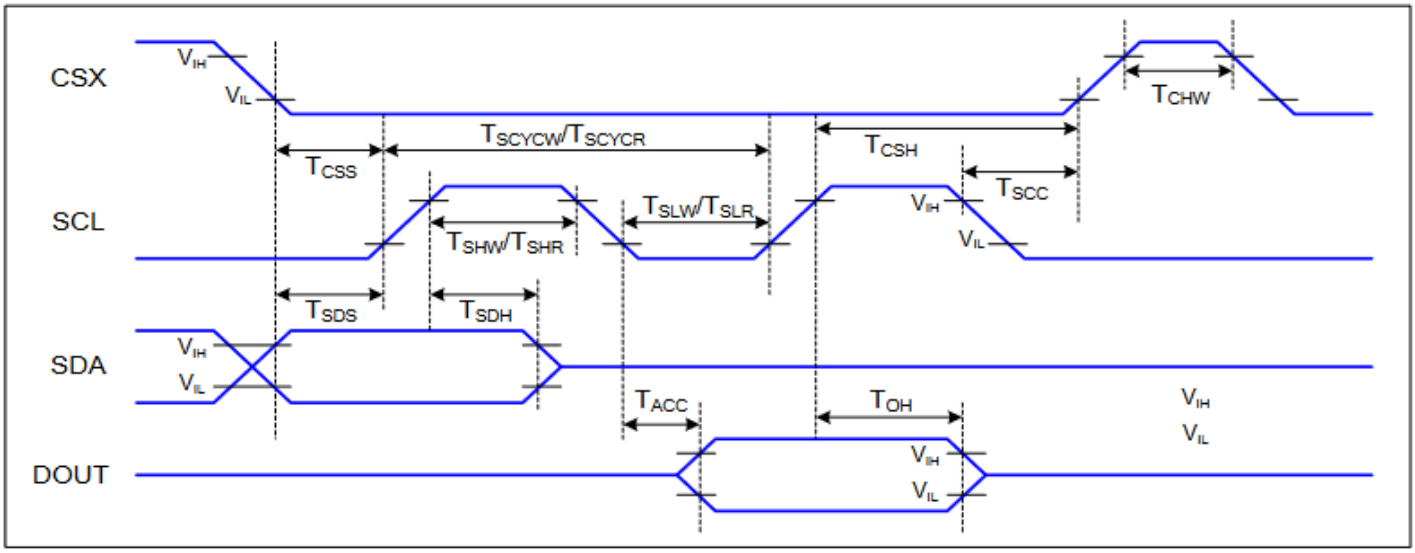
### 18-bit RGB Interface Characteristics




| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| HSYNC, VSYNC | $T_{SYNCS}$ | VSYNC, HSYNC Setup Time | 5 | - | ns | |
| ENABLE | $T_{ENS}$ | Enable Setup Time | 5 | - | ns | |
| | $T_{ENH}$ | Enable Hold Time | 5 | - | ns | |
| DOTCLK | PWDH | DOTCLK High-level Pulse Width | 15 | - | ns | |
| | PWDL | DOTCLK Low-level Pulse Width | 15 | - | ns | |
| | $T_{CYCD}$ | DOTCLK Cycle Time | 33 | - | ns | |
| | Trghr, Trghf | DOTCLK Rise/Fall time | - | 15 | ns | |
| DB | $T_{PDS}$ | PD Data Setup Time | 5 | - | ns | |
| | $T_{PDH}$ | PD Data Hold Time | 5 | - | ns | |

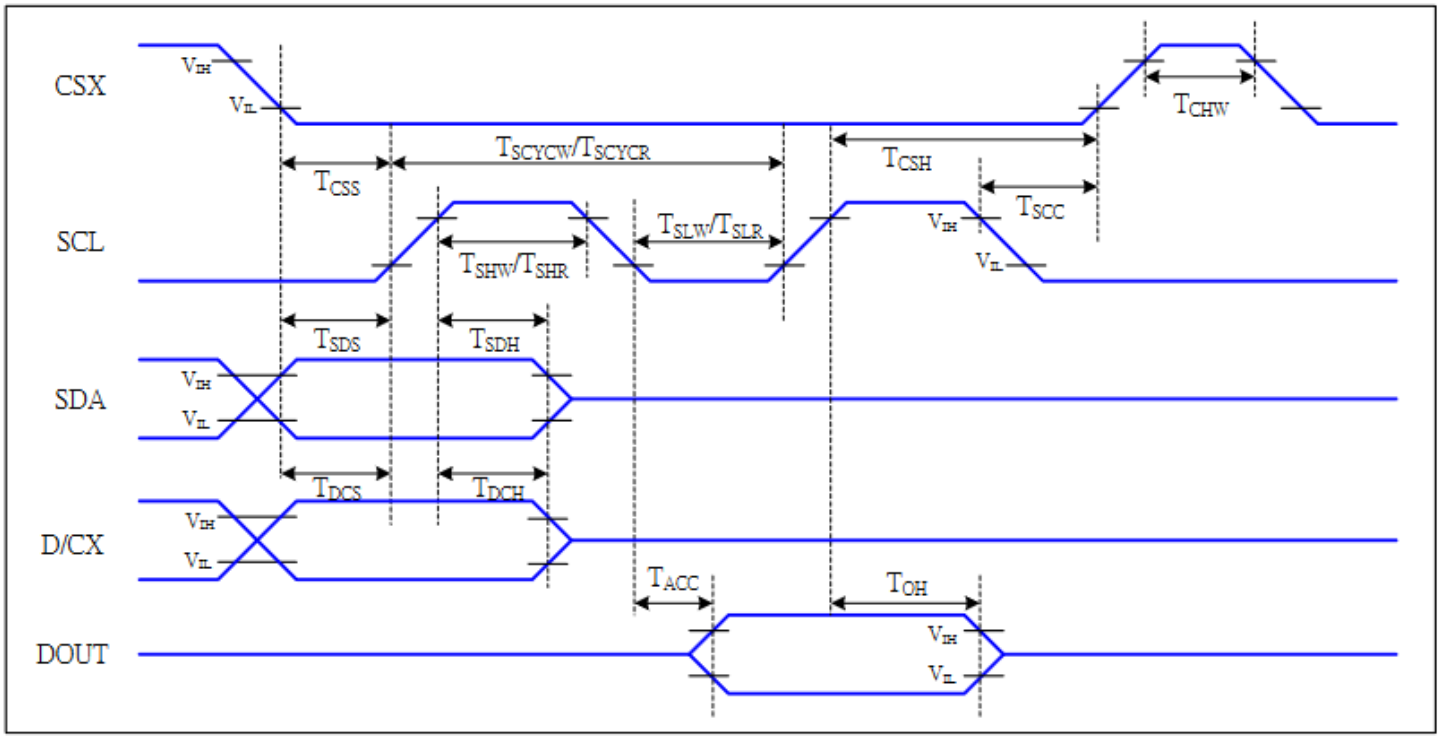
**Table 6 18/16 Bits RGB Interface Timing Characteristics**

**Serial Interface Characteristics (3-line serial)**




| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 60 | | ns | |
| | $T_{CHW}$ | Chip select “H” pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (Write) | 66 | | ns | |
| | $T_{SHW}$ | SCL “H” pulse width (Write) | 15 | | ns | |
| | $T_{SLW}$ | SCL “L” pulse width (Write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (Read) | 150 | | ns | |
| | $T_{SHR}$ | SCL “H” pulse width (Read) | 60 | | ns | |
| | $T_{SLR}$ | SCL “L” pulse width (Read) | 60 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |

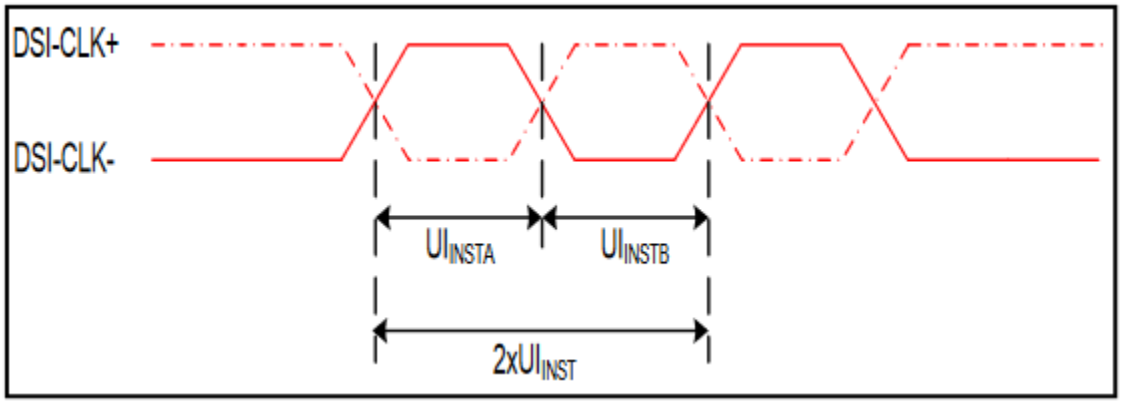
**Serial Interface Characteristics (4-line serial)**

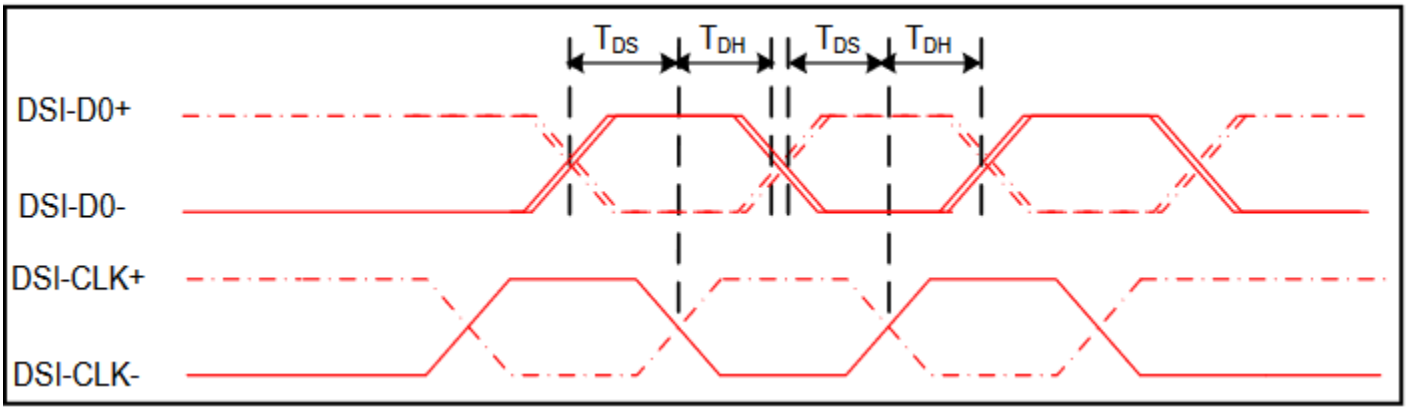



| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 65 | | ns | |
| | $T_{CHW}$ | Chip select “H” pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (Write) | 66 | | ns | -write command & data ram |
| | $T_{SHW}$ | SCL “H” pulse width (Write) | 15 | | ns | |
| | $T_{SLW}$ | SCL “L” pulse width (Write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (Read) | 150 | | ns | -read command & data ram |
| | $T_{SHR}$ | SCL “H” pulse width (Read) | 60 | | ns | |
| | $T_{SLR}$ | SCL “L” pulse width (Read) | 60 | | ns | |
| D/CX | $T_{DCS}$ | D/CX setup time | 10 | | ns | |
| | $T_{DCH}$ | D/CX hold time | 10 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |

## MIPI DSI Interface Characteristics

### High Speed Mode




**DSI timing characteristics**

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| DSI-CLK+/- | $2xUI_{INSTA}$ | Double UI instantaneous | 2.5 | 25 | ns | |
| DSI-CLK+/- | $UI_{INSTA}$ $UI_{INSTB}$ | UI instantaneous halfs | 1.25 | 12.5 | ns | UI = $UI_{INSTA}$= $UI_{INSTB}$ |
| DSI-Dn+/- | tDS | Data to clock setup time | 0.15 | - | UI | |
| DSI-Dn+/- | tDH | Data to clock hold time | 0.15 | - | UI | |

**Table 7 Mipi Interface- High Speed Mode Timing Characteristics**

**Low Power Mode**

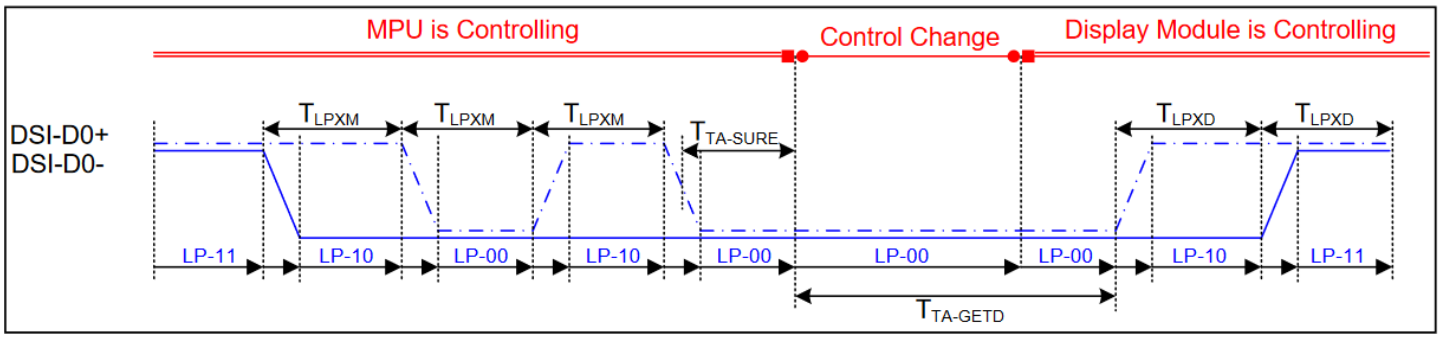



**Figure 6 Bus Turnaround (BTA) from display module to MPU Timing**

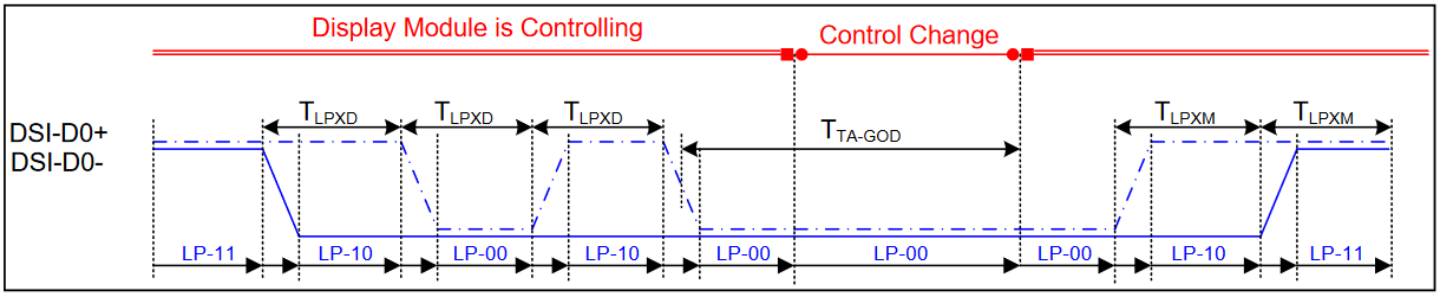



**Figure 7 Bus Turnaround (BTA) from MPU to display module Timing**

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| DSI-D0+/- | TLPXM | Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module | 50 | 75 | ns | Input |
| DSI-D0+/- | TLPXD | Length of LP-00,LP-01, LP-10 or LP-11 periods MPU→Display Module | 50 | 75 | ns | Output |
| DSI-D0+/- | TTA-SURED | Time-out before the MPU start driving | $T_{LPXD}$ | $2xT_{LPXD}$ | ns | Output |
| DSI-D0+/- | TTA-GETD | Time to drive LP-00 by display module | $5xT_{LPXD}$ | | ns | Input |
| DSI-D0+/- | TTA-GOD | Time to drive LP-00 after turnaround request-MPU | $4xT_{LPXD}$ | | ns | Output |

**Table 8 Mipi Interface Low Power Mode Timing Characteristics**

## DSI Burst Mode

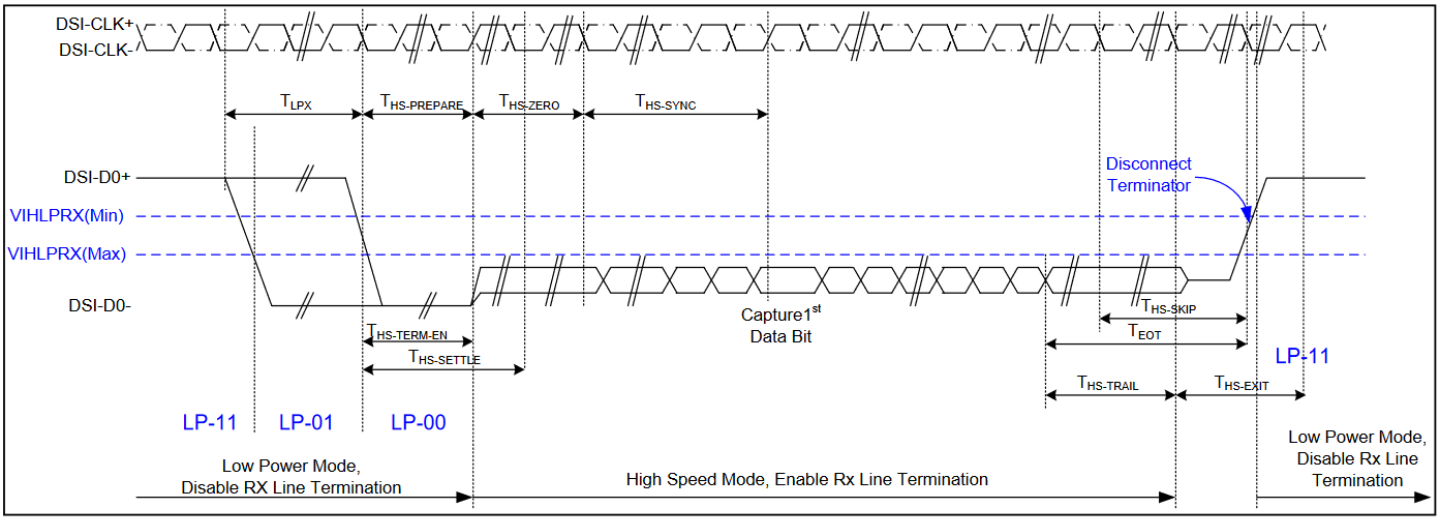



**Figure 7 Data lanes-Low Power Mode to/from High Speed Mode Timing**

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| Low Power Mode to High Speed Mode Timing | | | | | | |
| DSI-Dn+/- | TLPX | Length of any low power state period | 50 | - | ns | Input |
| DSI-Dn+/- | THS-PREPARE | Time to drive LP-00 to prepare for HS transmission | 40+4 UI | 85+6 UI | ns | Input |
| DSI-Dn+/- | THS-TERM-EN | Time to enable data receiver line termination measured from when Dn crosses VILMAX | - | 35+4 UI | ns | Input |
| DSI-Dn+/- | THS-PREPARE + THS-ZERO | THS-PREPARE + time to drive HS-0 before the sync sequence | 140+ 10UI | - | ns | Input |

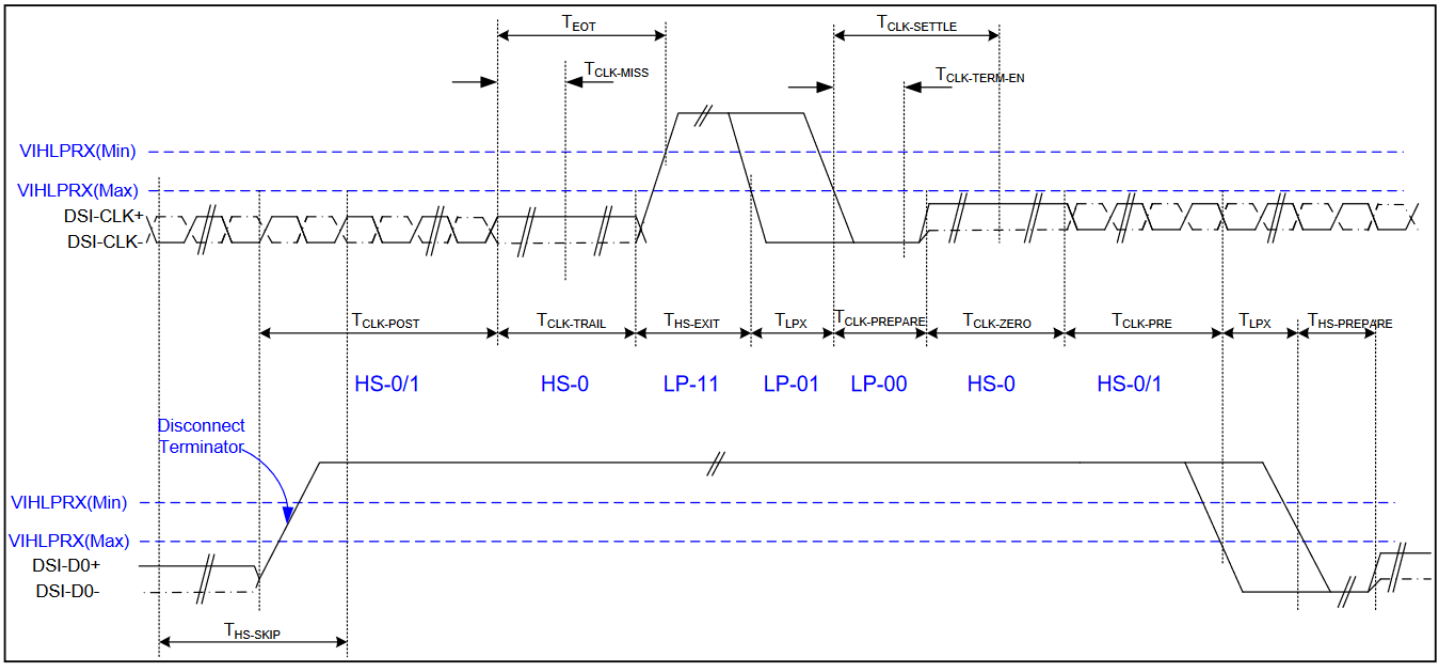
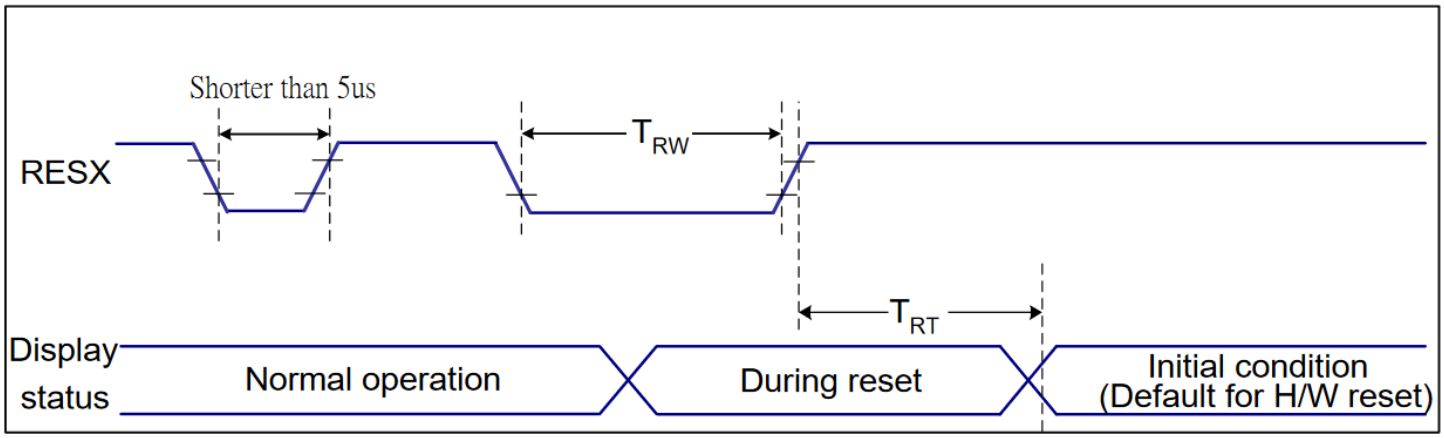



**Figure 8 Clock lanes- High Speed Mode to/from Low Power Mode Timing**

| High Speed Mode to/from Low Power Mode Timing | | | | | | |
|---|---|---|---|---|---|---|
| DSI-CLK+/- | TCLK-POS | Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode | 60+5 2UI | - | ns | Input |
| DSI-CLK+/- | TCLK-TRAIL | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns | Input |
| DSI-CLK+/- | THS-EXIT | Time to drive LP-11 after HS burst | 100 | - | ns | Input |
| DSI-CLK+/- | TCLK-PREPARE | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns | Input |
| DSI-CLK+/- | TCLK-TERM-EN | Time-out at clock lan display module to enable HS transmission | -- | 38 | ns | Input |
| DSI-CLK+/- | TCLK-PREPARE + TCLK-ZERO | Minimum lead HS-0 drive period before starting clock | 300 | - | ns | Input |
| DSI-CLK+/- | TCLK-PRE | Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode | 8UI | - | ns | Input |
| DSI-CLK+/- | TEOT | Time form start of TCLK-TRAIL period to start of LP-11 state | - | 105n s+12 UI | ns | Input |

**Reset Input Timing**




| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|---|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1, 5) | ms |
| | | | | 120(Note 1, 6, 7) | ms |

# Quality Information

| Test Item | Content of Test | Test Condition | Note |
|---|---|---|---|
| High Temperature storage | Endurance test applying the high storage temperature for a long time. | +80°C , 240hrs | 2 |
| Low Temperature storage | Endurance test applying the low storage temperature for a long time. | -30°C , 240hrs | 1,2 |
| High Temperature Operation | Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time. | +70°C , 240hrs | 2 |
| Low Temperature Operation | Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time. | -20°C , 240hrs | 1,2 |
| High Temperature / Humidity Storage | Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time. | +50°C , 90% RH , 120hrs | 1,2 |
| Thermal Shock resistance | Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress. | -20°C,60min -> 70°C,60min= 1 cycle<br>20 cycles | |
| Vibration test | Endurance test applying vibration to simulate transportation and use. | Frequency range:10Hz~50Hz<br>Acceleration of gravity:5G<br>X, Y, Z 30 min for each direction | 3 |
| Static electricity test | Endurance test applying electric static discharge. | Air: Vs=±4kV 150pF/330Ω, 5 Times<br>Contact: Vs= ±2kV 150pF/330Ω, 5 Times | |

**Note 1:** No condensation to be observed.
**Note 2:** Conducted after 4 hours of storage at 25°C, 0%RH.
**Note 3:** Test performed on product itself, not inside a container.