NEWHAVEN DISPLAY INTERNATIONAL

Product Specification

NHD-1.69-160128B

Graphic Color OLED Display

NHD-	Newhaven Display
1.69-	1.69" Diagonal Size
160128-	160 x 128 Pixels
B-	Model

Newhaven Display International, Inc.
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REACH Compliant

RoHS Compliant

NEWHAVEN DISPLAY INTERNATIONAL

Table of Contents

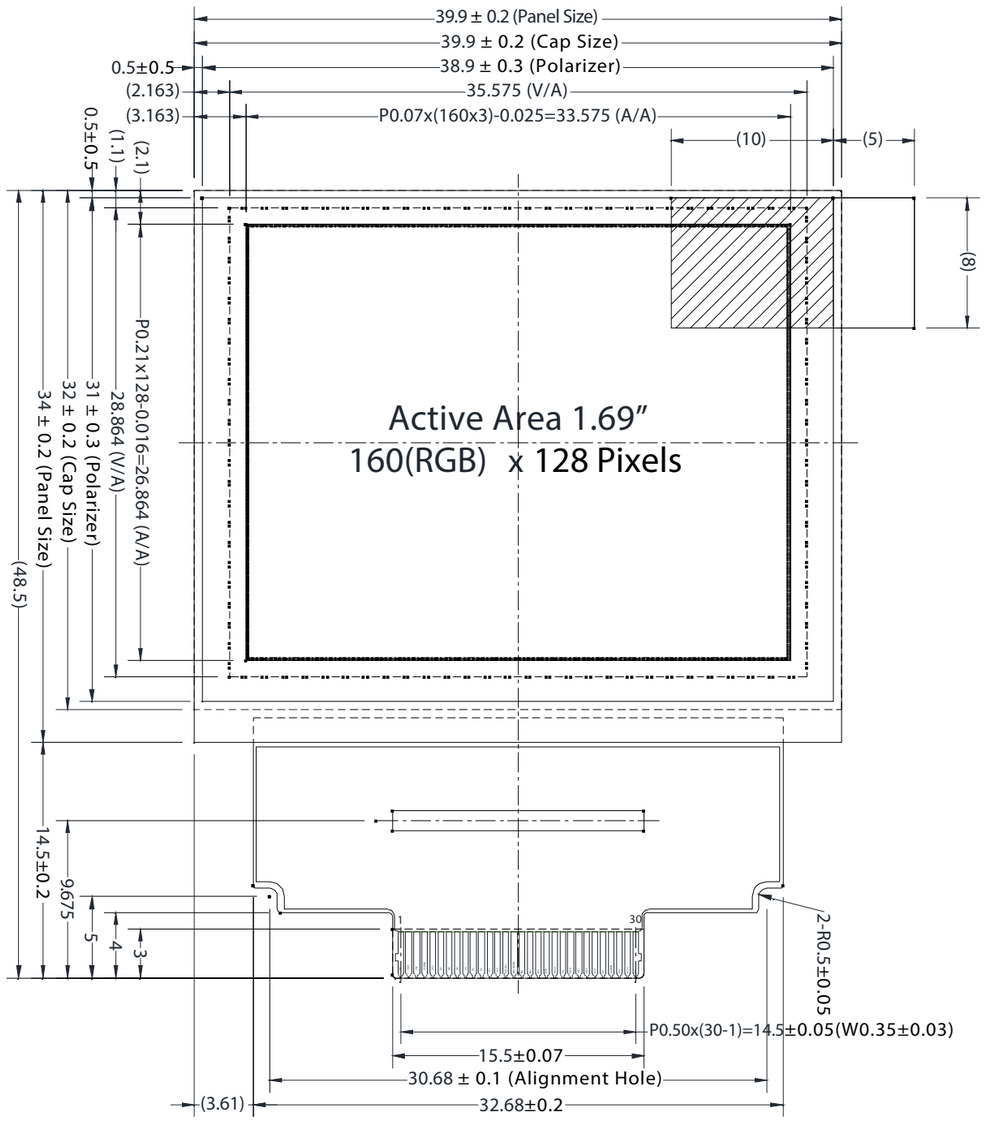
Additional Resources

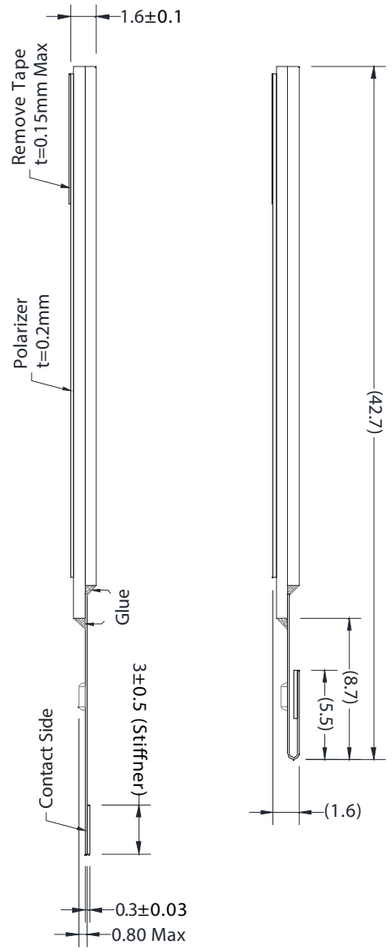
- **Support Forum:** https://support.newhavendisplay.com/hc/en-us/community/topics
- **GitHub:** https://github.com/newhavendisplay
- **Example Code:** https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** https://www.newhavendisplay.com/specs/precautions.pdf
- **Warranty / Terms & Conditions:** https://www.newhavendisplay.com/terms.html

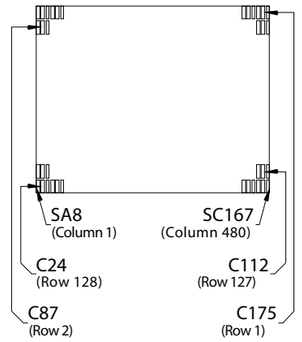
Document Revision History

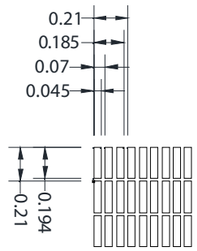
Revision	Date	Description	Changed By
-	04/29/2024	Initial Release	KL

Mechanical Drawing









Pixel Detail
Scale (10:1)

Pin	Symbol
1	NC
2	VLSS
3	VSL
4	VCOMH
5	VCC
6	D7
7	D6
8	D5
9	D4
10	D3
11	D2
12	D1
13	D0
14	E(RD#)
15	R/W#(WR#)
16	BS1
17	BS2
18	CS#
19	D/C#
20	RES#
21	FR
22	VDD
23	VSS
24	IREF
25	VCC
26	VP
27	VCOMH
28	VSL
29	VLSS
30	NC

Product Description: 1.69" 160x128 Color OLED

1. Driver IC: SSD1333
2. Interface: 8-bit 6800/8080 Parallel, 4-Wire SPI, I²C
3. Power Requirement: 3.3V
4. Optical Features: Full color, Full View
5. Recommended FFC Connector: 30pin 0.5mm pitch

Newhaven Display
NHD-1.69-160128B
Date Code
Part Label (type/format may vary)

Standard Tolerance:
(Unless otherwise specified)
Linear: ±0.3mm

NEWHAVEN DISPLAY INTERNATIONAL

Drawing/Part Number: NHD-1.69-160128B			Revision: 1A
Unless otherwise specified: • Dimensions are in Millimeters • Third Angle Projection	Drawn By: K. Lewis	Approved By: K. Lewis	
	Drawn Date: 04/29/2024	Approved Date: 04/29/2024	

Pin Description

Pin No.	Symbol	External Connection	Function Description
1	NC	-	No Connect
2	VLSS	Power Supply	Ground
3	VSL	-	Voltage for Low Level SEG Signal
4	VCOMH	-	Voltage for High Level COM Signal
5	VCC	Power Supply	Supply Voltage for OLED Panel (+14V)
6-13	D7-D0	MPU	**Parallel Interface:** 8-bit Bi-directional data bus **Serial Interface:** D0 - Synchronous Clock signal (SCLK) D1 - Serial Data Input signal (SDIN) - connect together with D2 **I²C Interface:** D0 - Synchronous Clock signal (SCL) D1 - Serial Data Input signal (SDAIN) D2 - Serial Data Output signal (SDAOUT)
14	E RD#	MPU	**6800 mode:** Enable signal. Falling edge triggered **8080 mode:** Active LOW Read signal
15	R/W# WR#	MPU	**6800 mode:** Read/Write signal. HIGH: Read, LOW: Write **8080 mode:** Active LOW Write signal
16	BS1	MPU	MPU Interface Select signal
17	BS2	MPU	MPU Interface Select signal
18	CS#	MPU	Active LOW Chip Select signal
19	D/C#	MPU	Data/Command Control signal. HIGH: Data, LOW: Command
20	RES#	MPU	Active LOW Reset signal
21	FR	MPU	RAM write synchronization signal (No Connect if not used)
22	VDD	Power Supply	Supply Voltage for Core Logic Circuit (+3V)
23	VSS	Power Supply	Ground
24	IREF	-	Current for SEG Brightness
25	VCC	Power Supply	Supply Voltage for OLED Panel (+14V)
26	VP	-	Voltage for SEG pre-charge
27	VCOMH	-	Voltage for High Level COM signal
28	VSL	-	Voltage for Low Level SEG signal
29	VLSS	Power Supply	Ground
30	NC	-	No Connect

Recommended display connector: 30pin 0.5mm pitch top contact FFC connector (Molex 52435-3072 or equivalent)

Interface Selection

MPU Interface Pin Selections and Assignment Summary

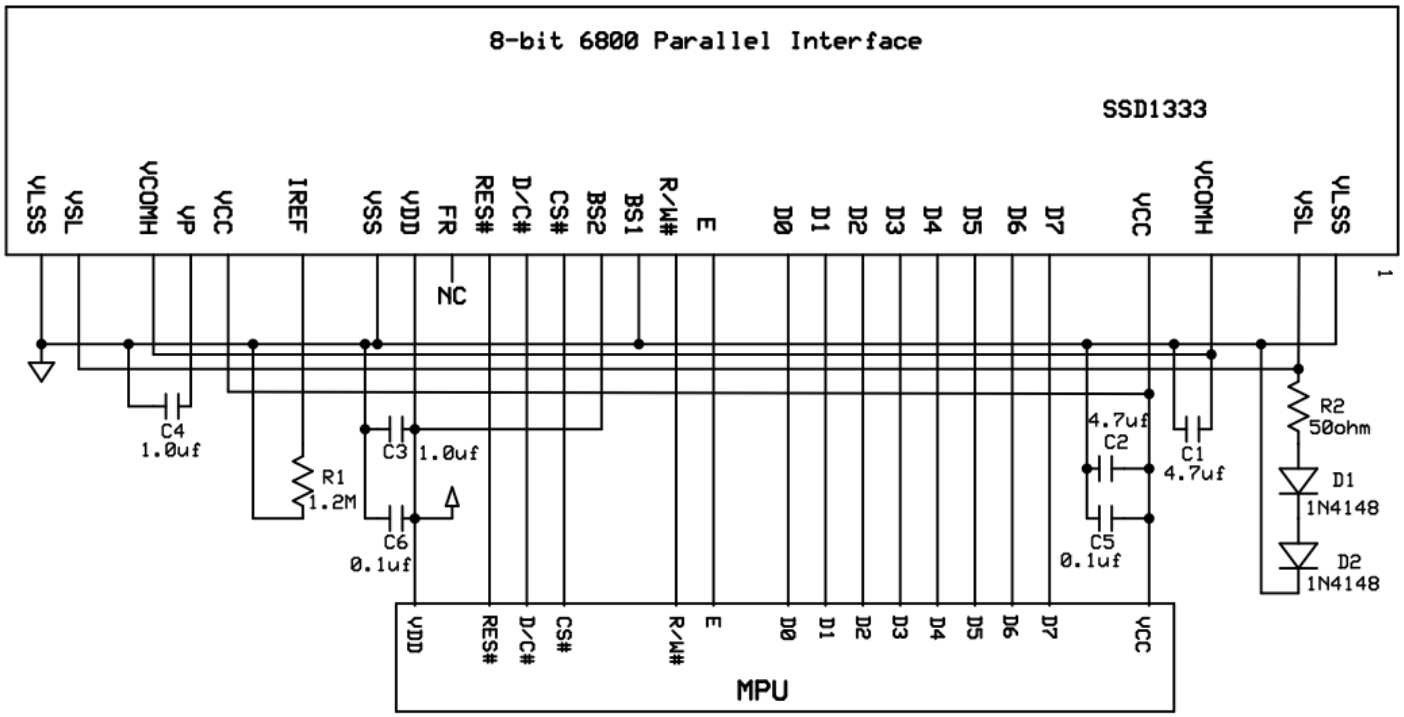
	6800 Parallel	8080 Parallel	4-Wire SPI	I²C
BS1	0	1	0	1
BS2	1	1	0	0

Bus Interface	Data/Command Interface								Control Signals				
	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
4-Wire SPI	Tie Low						SDIN	SCLK	Tie Low		CS#	D/C#	RES#
I²C	Tie Low					SDA_{OUT}	SDA_{IN}	SCL	Tie Low			SA0	RES#

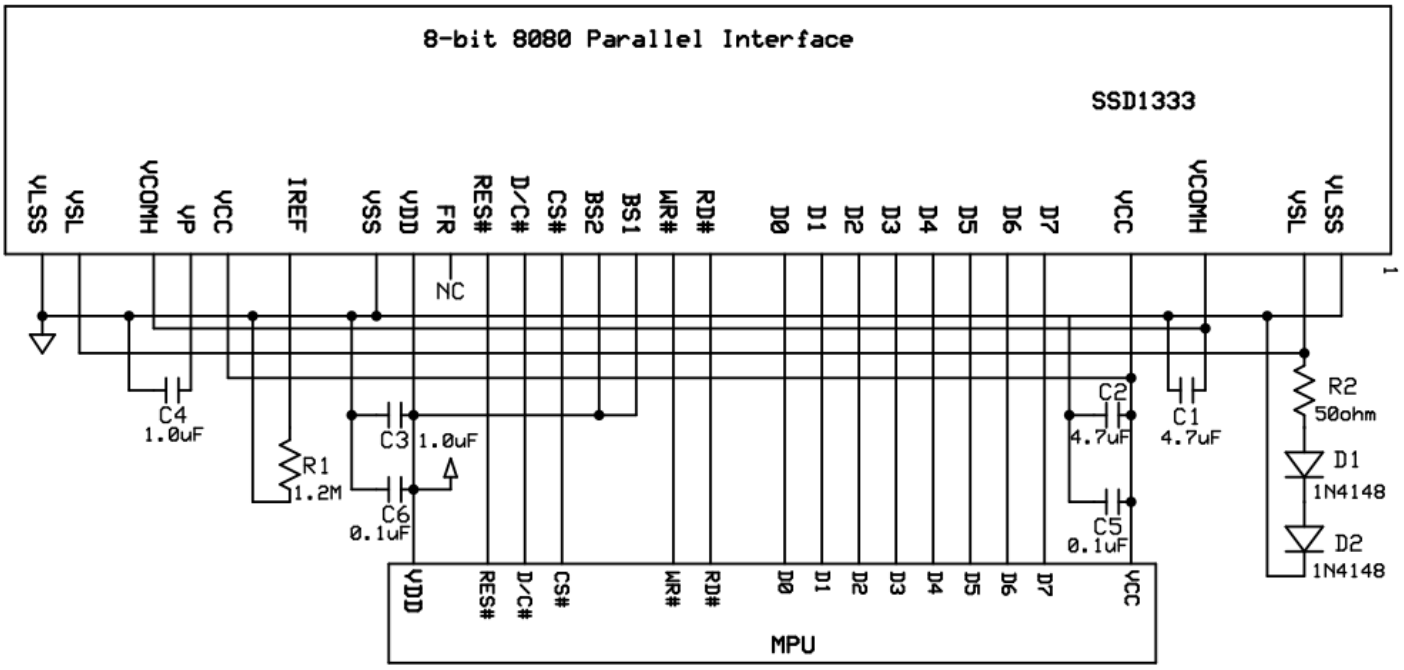
I²C Interface: SDA_{IN} and SDA_{OUT} are tied together and serve as SDA. The SDA_{IN} pin must be connected to act as SDA. The SDA_{OUT} pin may be disconnected. When SDA_{OUT} pin is disconnected, the acknowledgement signal will be ignored in the I²C-bus.

Wiring Diagram

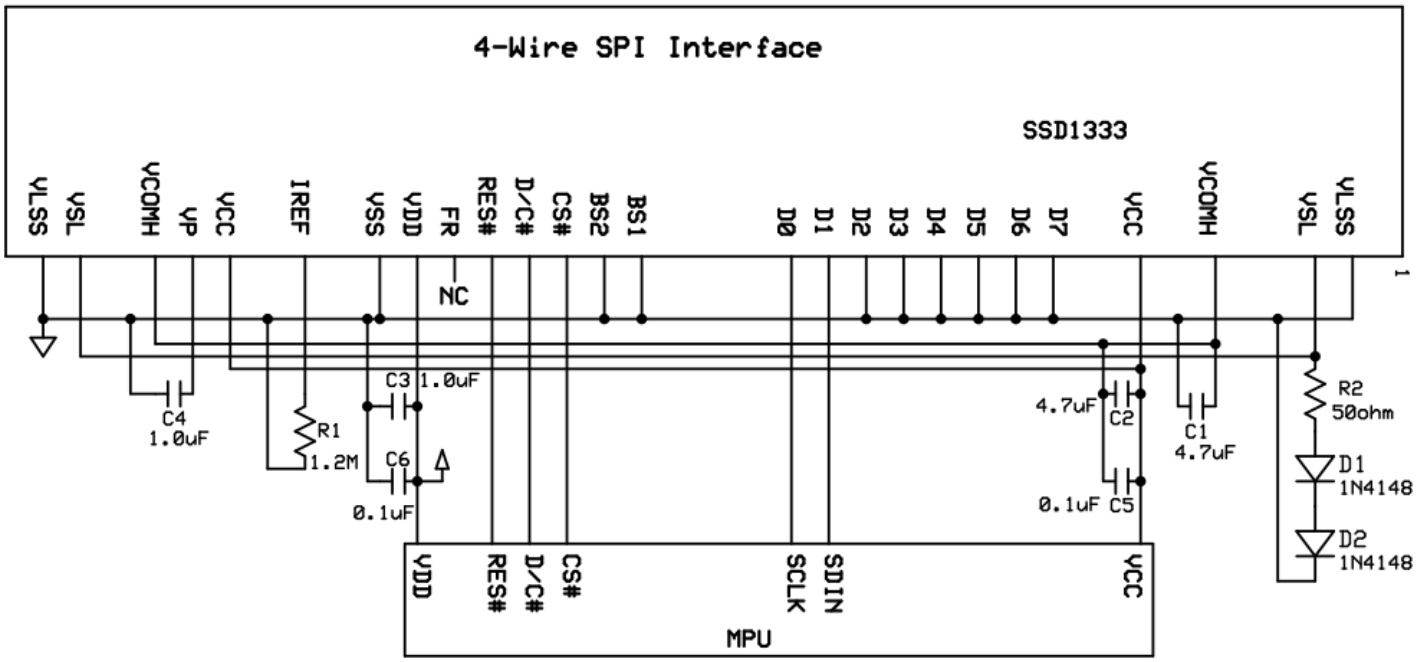
6800 Parallel Interface



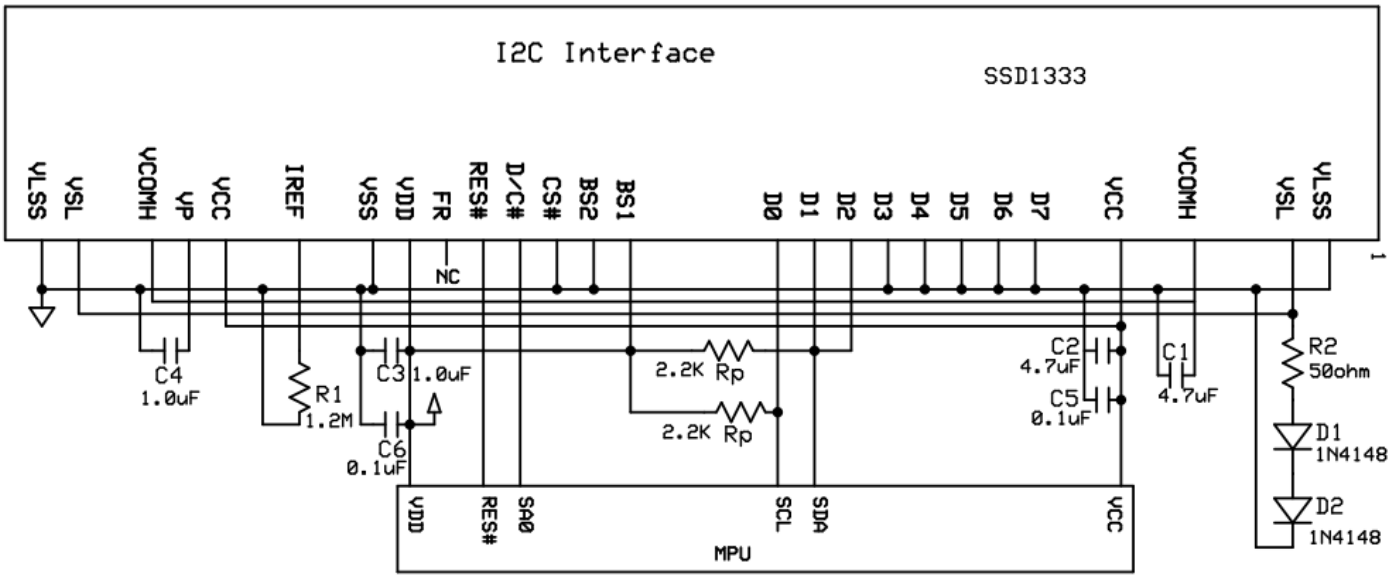
8080 Parallel Interface



4-Wire SPI Interface



I²C Interface



Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T_{OP}	Absolute Max	-40	-	+70	°C
Storage Temperature Range	T_{ST}	Absolute Max	-40	-	+85	°C
Supply Voltage for Logic	V_{DD}	-	1.65	3.3	3.5	V
Supply Voltage for Display	Vcc	-	13.5	14	14.5	V
Supply Current (Logic)	I_{DD}	-	-	840	930	µA
Supply Current (Display)	Icc	V_{DDH}=14V, 50% ON	-	26.4	33.0	mA
		V_{DDH}=14V, 100% ON	-	44.6	55.8	mA
Sleep mode Current	$I_{DD, SLEEP}$	-	-	-	10	µA
"H" Level input	V_{IH}	-	0.8*V_{DD}	-	V_{DD}	V
"L" Level input	V_{IL}	-	V_{SS}	-	0.2*V_{DD}	V
"H" Level output	V_{OH}	-	0.9*V_{DD}	-	V_{DD}	V
"L" Level output	V_{OL}	-	V_{SS}	-	0.1*V_{DD}	V

Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Optimal Viewing Angles	Top	φY+	-	-	85	-	°
	Bottom	φY-		-	85	-	°
	Left	θX-		-	85	-	°
	Right	θX+		-	85	-	°
Contrast Ratio		CR	-	-	>10,000:1	-	-
Response Time	Rise	T_R	-	-	10	-	µs
	Fall	T_F		-	10	-	µs
Brightness		L_V	-	80	100	-	cd/m²
Lifetime		-	80cd/m², T_{OP} =25°C, 50% Checkerboard	21,000	-	-	Hrs.
Chromaticity	Red	X_R	-	0.62	0.66	0.70	-
		Y_R	-	0.28	0.32	0.36	-
	Green	X_G	-	0.24	0.28	0.32	-
		Y_G	-	0.60	0.64	0.68	-
	Blue	X_B	-	0.10	0.14	0.18	-
		Y_B	-	0.16	0.21	0.26	-
	White	X_W	-	0.26	0.30	0.34	-
		Y_W	-	0.29	0.33	0.37	-

Note: Lifetime at typical temperature is based on accelerated high-temperature operation. Lifetime is tested at average 50% pixels on and is rated as Hours until **Half-Brightness**. The Display OFF command can be used to extend the lifetime of the display.
Luminance of active pixels will degrade faster than inactive pixels. Residual (burn-in) images may occur. To avoid this, every pixel should be illuminated uniformly.

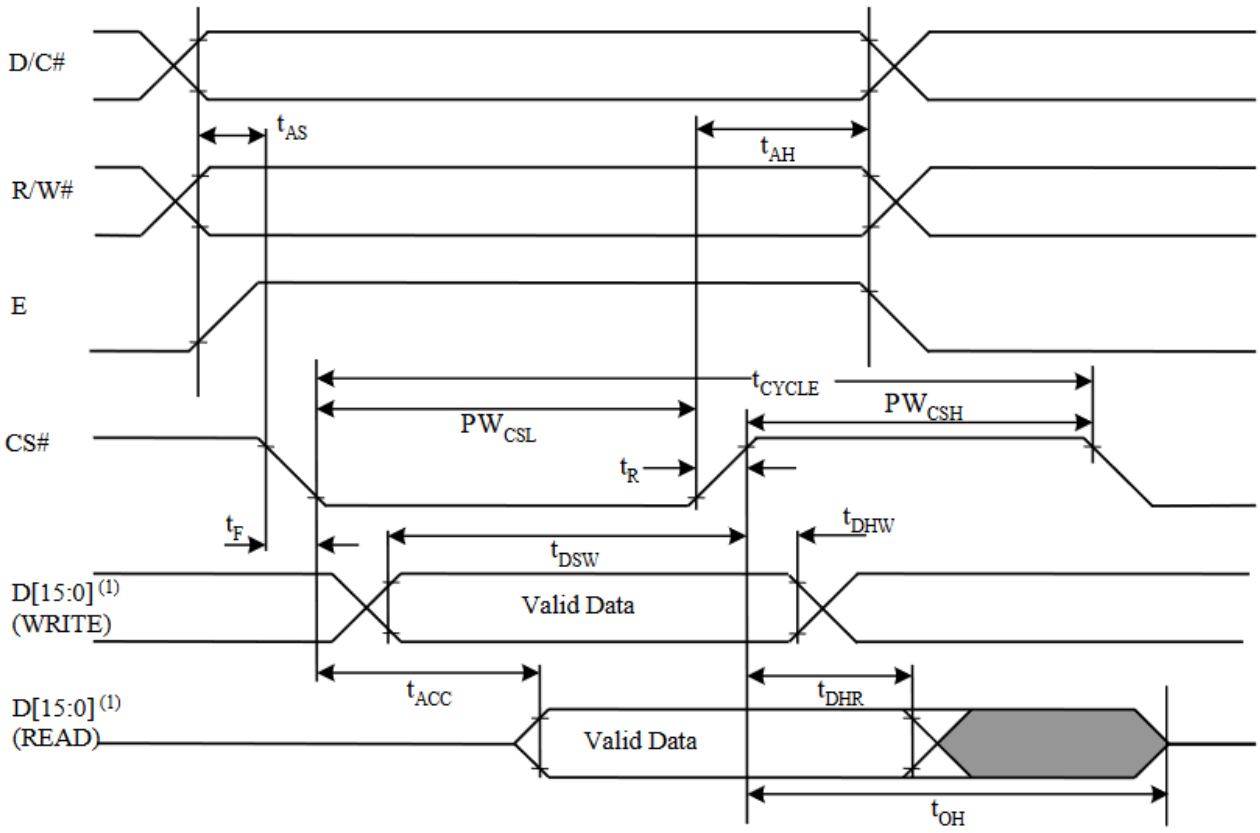
Controller information

Built-in SSD1333 Controller: https://support.newhavendisplay.com/hc/en-us/articles/11256414111767-SSD1333

Timing Characteristics

6800-Series MCU Parallel Interface:

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (write)	300	-	-	ns
t_{AS}	Address Setup Time	24	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	160 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

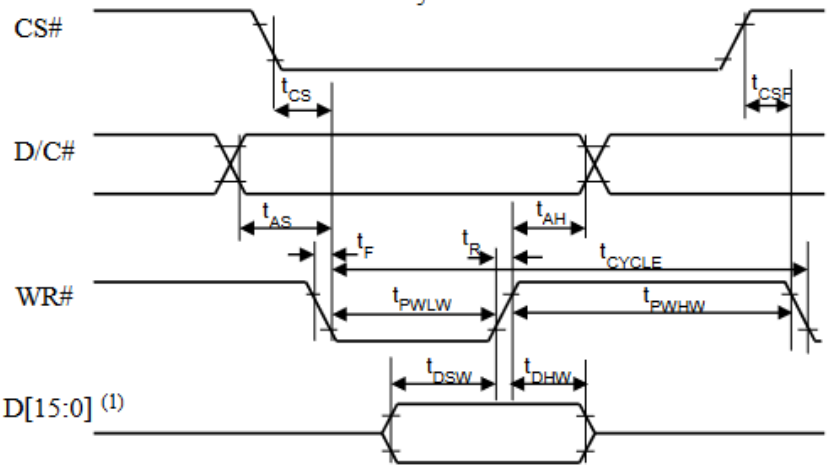


Note
(1) when 8 bit used: D[7:0] instead; when 16 bit used: D[15:0] instead.

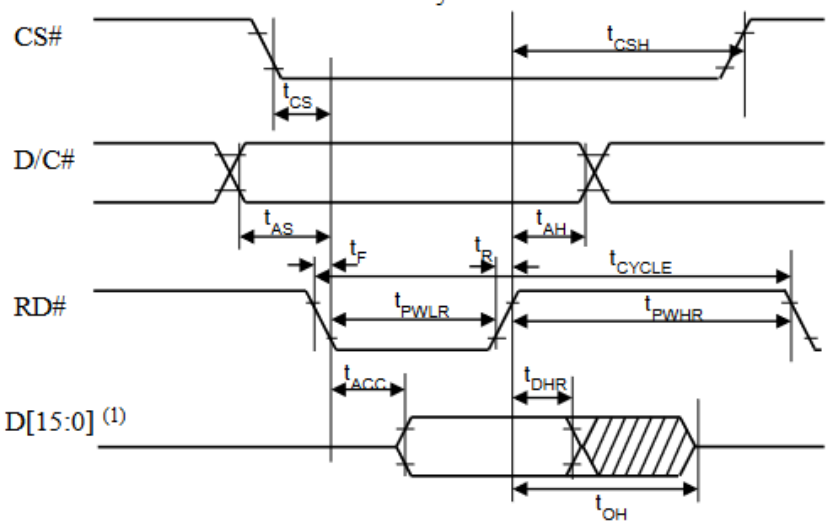
8080-Series MCU Parallel Interface:

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time (write)	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	46	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	160	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Write cycle



Read cycle

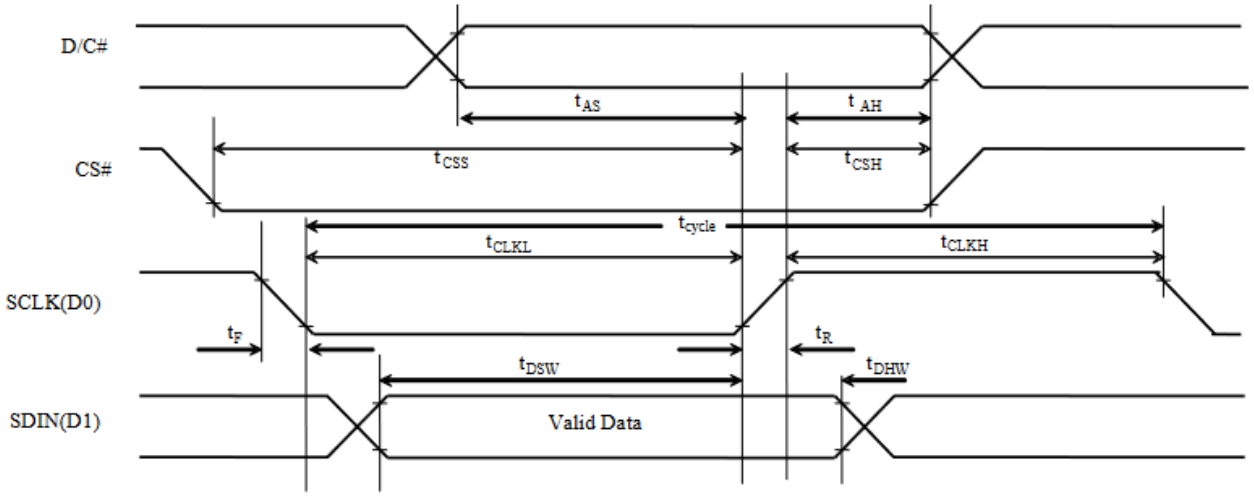


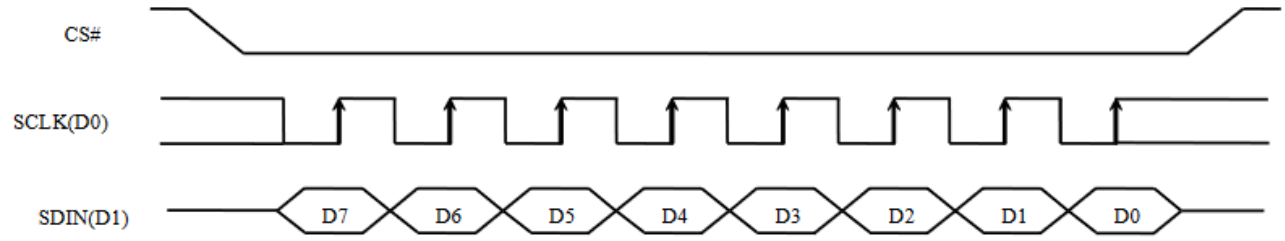
Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead.

4-wire SPI:

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	42	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	25	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns





I2C:

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA $_{OUT}$" pin)	0	-	-	ns
	Data Hold Time (for "SDA $_{IN}$" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

Figure 9-5 : I²C interface Timing characteristics

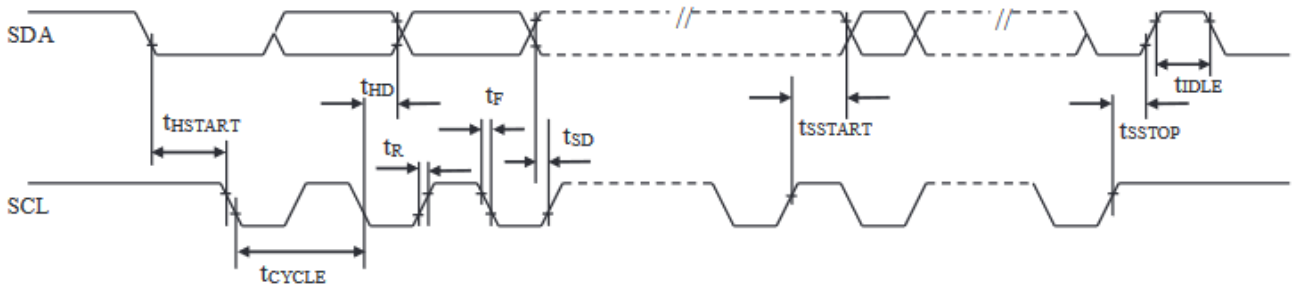


Table of Commands

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	15	0	0	0	1	0	1	0	1	Set Column Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=175d] Ranges from 0 to 175
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	75	0	1	1	1	0	1	0	1	Set Row Address	A[7:0]: Start Address. [reset=0] B[7:0]: End Address. [reset=175d] Ranges from 0 to 175
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	5C	0	1	0	1	1	1	0	0	Write RAM Command	Enable MCU to write Data into RAM
0	5D	0	1	0	1	1	1	0	1	Read RAM Command	Enable MCU to read Data from RAM
0	A0	1	0	1	0	0	0	0	0	Set Re-map / Color Depth (Display RAM to Panel)	A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Column address 0 is mapped to SEG0 [reset] A[1]=1b, Column address 175 is mapped to SEG0 A[2]=0b, Color sequence: A → B → C [reset] A[2]=1b, Color sequence is swapped: C → B → A A[3]=0b, Reserved [reset] A[3]=1b, Reserved A[4]=0b, Scan from COM0 to COM[N –1] [reset] A[4]=1b, Scan from COM[N-1] to COM0. Where N is the Multiplex ratio. A[5]=0b, Disable COM Split Odd Even A[5]=1b, Enable COM Split Odd Even [reset] A[7:6] Set Color Depth, 00b: 256color 01b: 65k color [reset] 10b: 262k color 11b Pseudo 262k color, 16-bit format 2 Refer to Product Preview Table 6-7 for details
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 1	A1 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set vertical scroll by RAM from 0~175. [reset=00h]
0 1	A2 A[7:0]	1 A_7	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by Row from 0-175. [reset=00h]
0	A4~A7	1	0	1	0	0	1	X_1	X_0	Set Display Mode	A4h: All OFF A5h: All ON (All pixels have GS63) A6h : Reset to normal display [reset] A7h: Inverse Display (GS0 -> GS63, GS1 -> GS62, ...)
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Sleep mode ON/OFF	AEh = Sleep mode On (Display OFF) AFh = Sleep mode OFF (Display ON)
0 1	B1 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Reset (Phase 1) / Pre-charge (Phase 2) period	A[3:0] Phase 1 period of 2~30 DCLK(s) clocks [reset=0100b] A[3:0]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 = 30DCLKs A[7:4] Phase 2 period of 2~30 DCLK(s) clocks [reset=1000b] A[7:4]: 0 invalid 1 = 2 DCLKs 2 = 4 DCLKs : 15 =30DCLKs Note (1) 0 DCLK is invalid in phase 1 & phase 2

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B3	1	0	1	1	0	0	1	1	Front Clock Divider (DivSet)/ Oscillator Frequency	A[3:0] [reset=0000b], divide by DIVSET where A[7:4] Oscillator frequency, frequency increases as level increases [reset=1001b]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	B6	1	0	1	1	0	1	0	0	Set Second Pre-charge Period	A[3:0] Set Second Pre-charge Period 0000b invalid 0001b 1 DCLKS 0010b 2 DCLKS .... 1000 8 DCLKS [reset] .... 1111 15 DCLKS
1	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		
0	B8	1	0	1	1	1	0	0	0	Master Look Up Table for Gray Scale Pulse width (Color A,B,C)	The next 63 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d). A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A62[7:0]: Gamma Setting for GS62, A63[7:0]: Gamma Setting for GS63 **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS62 < Setting of GS63 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input only, color A, B, C will follow the master LUT. (5) When command BCh is input, it selects individual LUT for color A, GS1~31A; When command BDh is input, it selects individual LUT for color C, GS1~31C (6) To select individual LUT for color B, A and C, command B8h should be input before command BCh and BDh,
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A62[7:0]	$A62_7$	$A62_6$	$A62_5$	$A62_4$	$A62_3$	$A62_2$	$A62_1$	$A62_0$		
1	A63[7:0]	$A63_7$	$A63_6$	$A63_5$	$A63_4$	$A63_3$	$A63_2$	$A63_1$	$A63_0$		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	B9	1	0	1	1	1	0	0	1	Use Built-in Linear LUT [reset= linear]	Reset to default Look Up Table: Color A: GS1A = 0 DCLK; GS2A = 4 DCLK; GS3A = 8 DCLK; ...; GS31A = 120 DCLK Color B: GS1B = 0 DCLK; GS2B = 2 DCLK; GS3B = 4 DCLK; ...; GS62B = 122 DCLK; GS63B = 124 DCLK Color C: GS1C = 0 DCLK; GS2C = 4 DCLK; GS3C = 8 DCLK; ...; GS31C = 120 DCLK
0	BB	1	0	1	1	1	0	1	1	Set Pre-charge voltage	Set pre-charge voltage level.[reset = 01111b]
1	A[4:0]	0	0	0	A_4	A_3	A_2	A_1	A_0		A[4:0] / Hex code / pre-charge voltage: 00000 / 00h / 0.10 x V_{CC} : / : / : 10111 / 17h / 0.40 x V_{CC} [reset] : / : / : 11111 / 1Fh / 0.5133 x V_{CC} **Note** (1)Pre-charge voltage level must be smaller than COM deselect voltage level
0	BC	1	0	1	1	1	1	0	0	Individual Look Up Table for Gray Scale Pulse width (Color A)	The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color A. A1[7:0]: Gamma Setting for GS1A, A2[7:0]: Gamma Setting for GS2A, : A30[7:0]: Gamma Setting for GS30A, A31[7:0]: Gamma Setting for GS31A **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for color A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A30[7:0]	$A30_7$	$A30_6$	$A30_5$	$A30_4$	$A30_3$	$A30_2$	$A30_1$	$A30_0$		
1	A31[7:0]	$A31_7$	$A31_6$	$A31_5$	$A31_4$	$A31_3$	$A31_2$	$A31_1$	$A31_0$		

Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	BD	1	0	1	1	1	1	0	1	Individual Look Up Table for Gray Scale Pulse width (Color C)	The next 31 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d) for color C. A1[7:0]: Gamma Setting for GS1C, A2[7:0]: Gamma Setting for GS2C, : A30[7:0]: Gamma Setting for GS30C, A31[7:0]: Gamma Setting for GS31C **Note** (1) 0 ≤ Setting of GS1 < Setting of GS2 < Setting of GS3..... < Setting of GS30 < Setting of GS31 (2) GS0 does not has pre-charge and current drive stages. (3) GS1 can be set as only pre-charge but no current drive stage by input gamma setting for GS1 equals 0. (4) When command B8h is input, it selects one LUT for color A, B and C. i.e. GS1~31A, GS1~63B and GS1~31C are updated. (5) Command B8h should be input before command BCh and BDh to select individual LUT for color B, A and C.
1	A1[7:0]	$A1_7$	$A1_6$	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$		
1	A2[7:0]	$A2_7$	$A2_6$	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	.	.	.	.	.	.	.	.	.		
1	A30[7:0]	$A30_7$	$A30_6$	$A30_5$	$A30_4$	$A30_3$	$A30_2$	$A30_1$	$A30_0$		
1	A31[7:0]	$A31_7$	$A31_6$	$A31_5$	$A31_4$	$A31_3$	$A31_2$	$A31_1$	$A31_0$		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Set COM deselect voltage level [reset = 05h] A[2:0] / Hex code / V_{COMH} 000 / 00h / 0.72 x V_{CC} : / : / : 101 / 05h / 0.82 x V_{CC} [reset] : / : / : 111 / 07h / 0.86 x V_{CC}
1	A[2:0]	0	0	0	0	0	A_2	A_1	A_0		
0	C1	1	1	0	0	0	0	0	1	Set Contrast Current for Color A,B,C	A[7:0] Contrast Value Color A [reset=7Fh] B[7:0] Contrast Value Color B [reset=7Fh] C[7:0] Contrast Value Color C [reset=7Fh]
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
1	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
1	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		
0	C7	1	1	0	0	0	1	1	1	Master Contrast Current Control	A[3:0] : 0000b reduce output currents for all colors to 1/16 0001b reduce output currents for all colors to 2/16 .... 1110b reduce output currents for all colors to 15/16 1111b no change [reset]
1	A[3:0]	0	0	0	0	A_3	A_2	A_1	A_0		
0	CA	1	1	0	0	1	0	1	0	Set MUX Ratio	A[6:0] MUX ratio 4MUX ~ 176MUX, [reset=175] (Ranges from 3 to 175)
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	FD	1	1	1	1	1	1	0	1	Set Command Lock	A[7:0]: MCU protection status [reset = 12h] A[7:0] = 12h, Unlock OLED driver IC MCU interface from entering command [reset] A[7:0] = 16h, Lock OLED driver IC MCU interface from entering command **Note** (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command.
1	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

Note
(1) "*" stands for "Don't care".

Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Test the endurance of the display at high storage temperature.	+85°C, 240hrs	2
Low Temperature storage	Test the endurance of the display at low storage temperature.	-40°C, 240hrs	1,2
High Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature.	+70°C, 240hrs	2
Low Temperature Operation	Test the endurance of the display by applying electric stress (voltage & current) at low temperature.	-40°C, 240hrs	1,2
High Temperature / Humidity Operation	Test the endurance of the display by applying electric stress (voltage & current) at high temperature with high humidity.	+60°C, 90% RH, 120hrs	1,2
Thermal Shock resistance	Test the endurance of the display by applying electric stress (voltage & current) during a cycle of low and high temperatures.	-40°C,60m-> 85°C,60min = 1 cycle 24 cycles	
Vibration test	Test the endurance of the display by applying vibration to simulate transportation and use.	10-22Hz, 15mm amplitude. 22-500Hz, 1.5G 30min in each of 3 directions X,Y,Z	3
Atmospheric Pressure test	Test the endurance of the display by applying atmospheric pressure to simulate transportation by air.	115mbar, 40hrs	3
Static electricity test	Test the endurance of the display by applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.
Note 2: Conducted after 2 hours of storage at 25°C, 0%RH.
Note 3: Test performed on product itself, not inside a container.
Evaluation Criteria:
1: Display is fully functional during operational tests and after all tests, at room temperature.
2: No observable defects.
3: Luminance >50% of initial value.
4: Current consumption within 50% of initial value